# Electronics for SLHC

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"Prediction is very difficult, especially if it's about the future"

*Niels Bohr*

# Outline

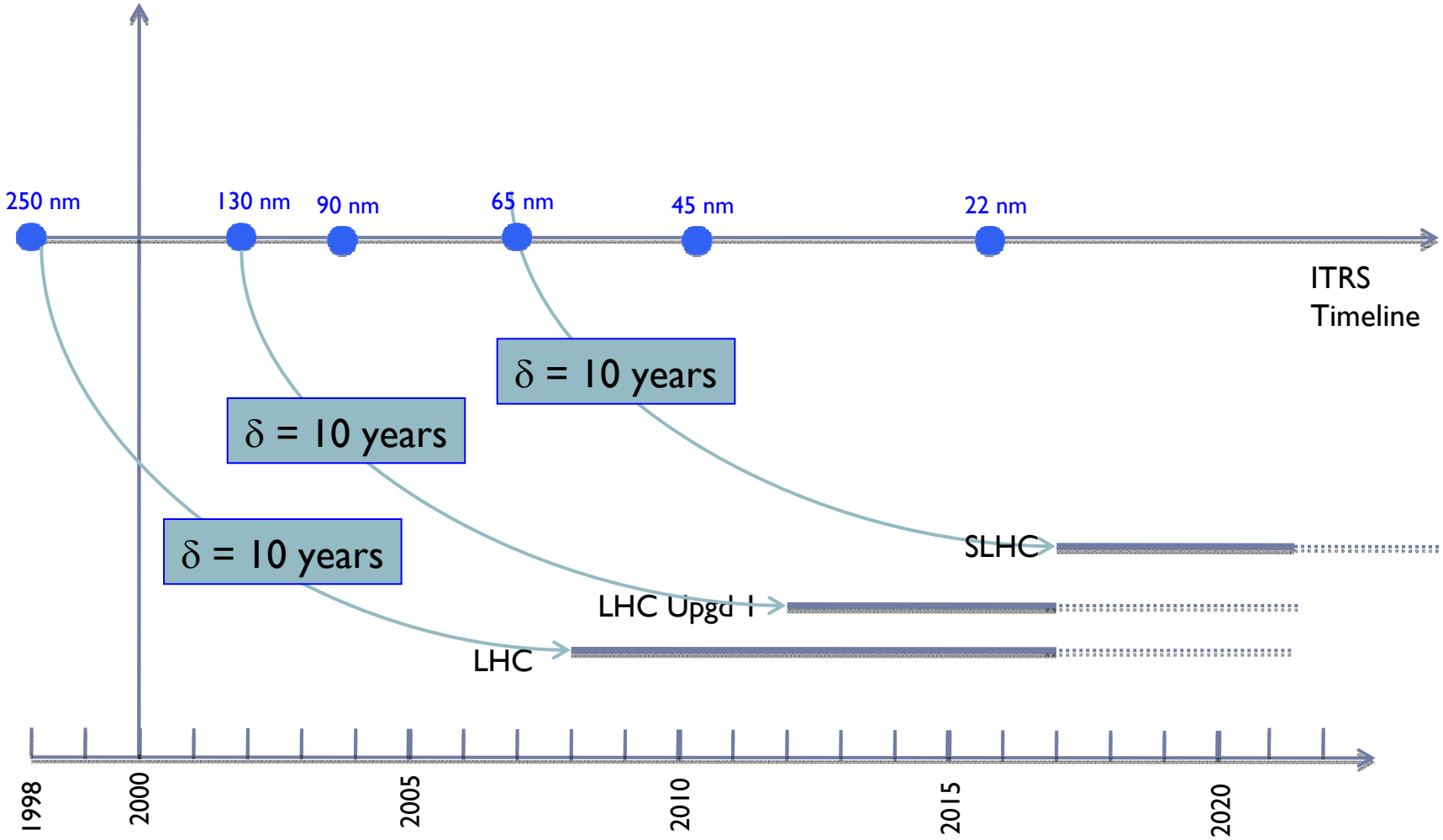
- The SLHC schedule against ITRS roadmap
  - What will industry be supplying at the time of SLHC?
- What will be SLHC biggest problem (in electronics)?
  - Radiation hardness
  - Density of channels in trackers
    - What type of problem is this?
      - Logic density?
      - Interconnect?
      - Data transmission?
  - Power dissipation and material budget

# ITRS Roadmap

| ITRS | 2004 | 2007 | 2010 | 2013 | 2016 |
|---|---|---|---|---|---|
| Technology Node [nm] | 90 | 65 | 45 | 32 | 22 |
| Transistor count [Mtr] | | | 1500 | 3092 | 6184 |
| Transistor Density [Mtr/cm2] | 77 | 154 | 309 | 617 | 1235 |
| Chip Size | 140 | | | | 280 |
| Clock freq [GHz] | 3 | | 15 | | 53 |
| Vdd | 1.2 | 1.1 | 1.0 | 0.9 | 0.7 |
| DRAM half pitch | 90 | 65 | 54 | 32 | 22 |
| Signal IO Pads | 512 | 1024 | 1024 | 1024 | 1024 |
| Power Pads | 1024 | | | | 2048 |

from International Technology Roadmap for Semiconductors 2003

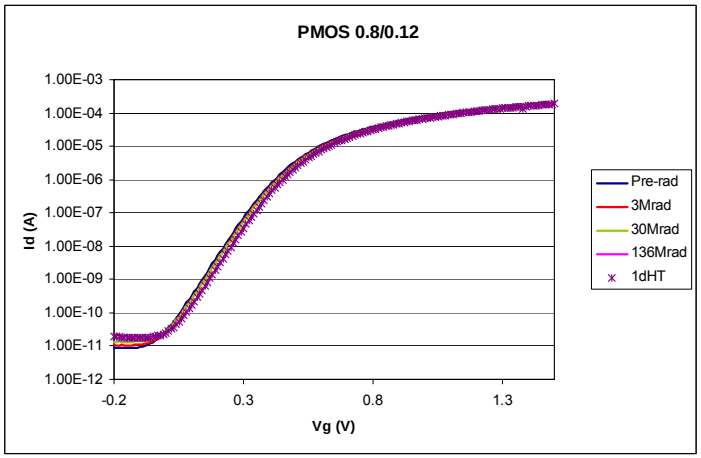
# Perspectives

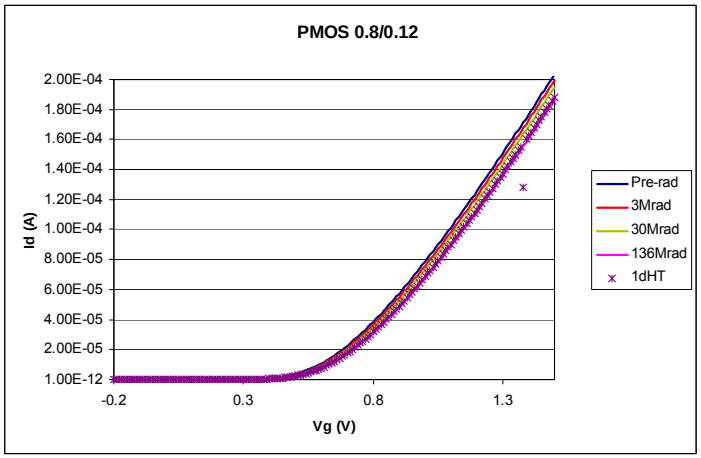


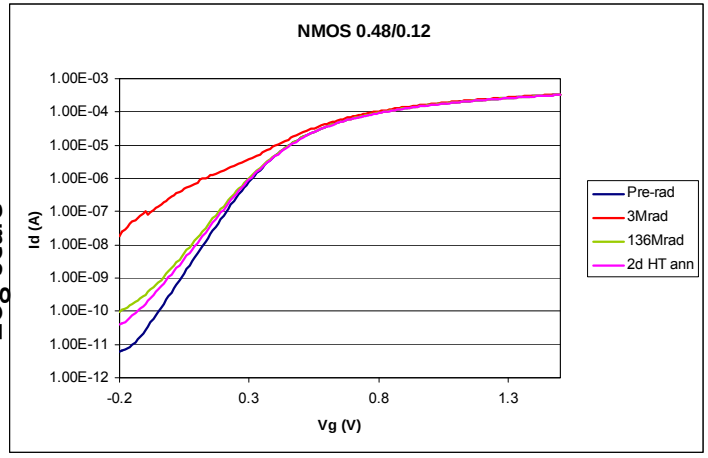
# Will radiation be a problem?

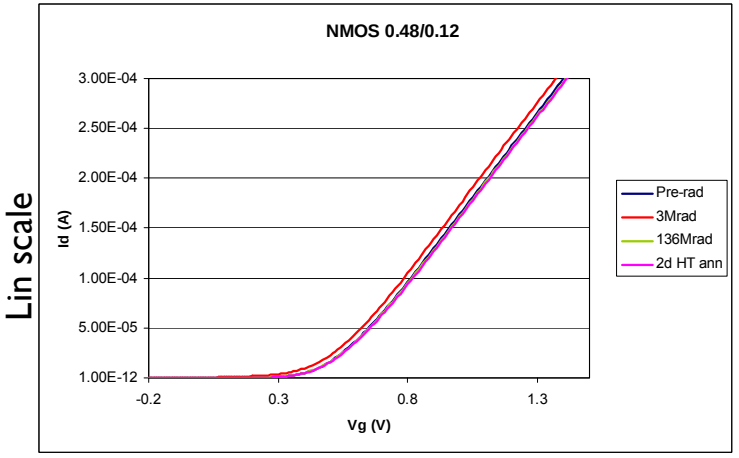
# 130 nm TID performance

## Core NMOS transistors, foundry "A", linear layout



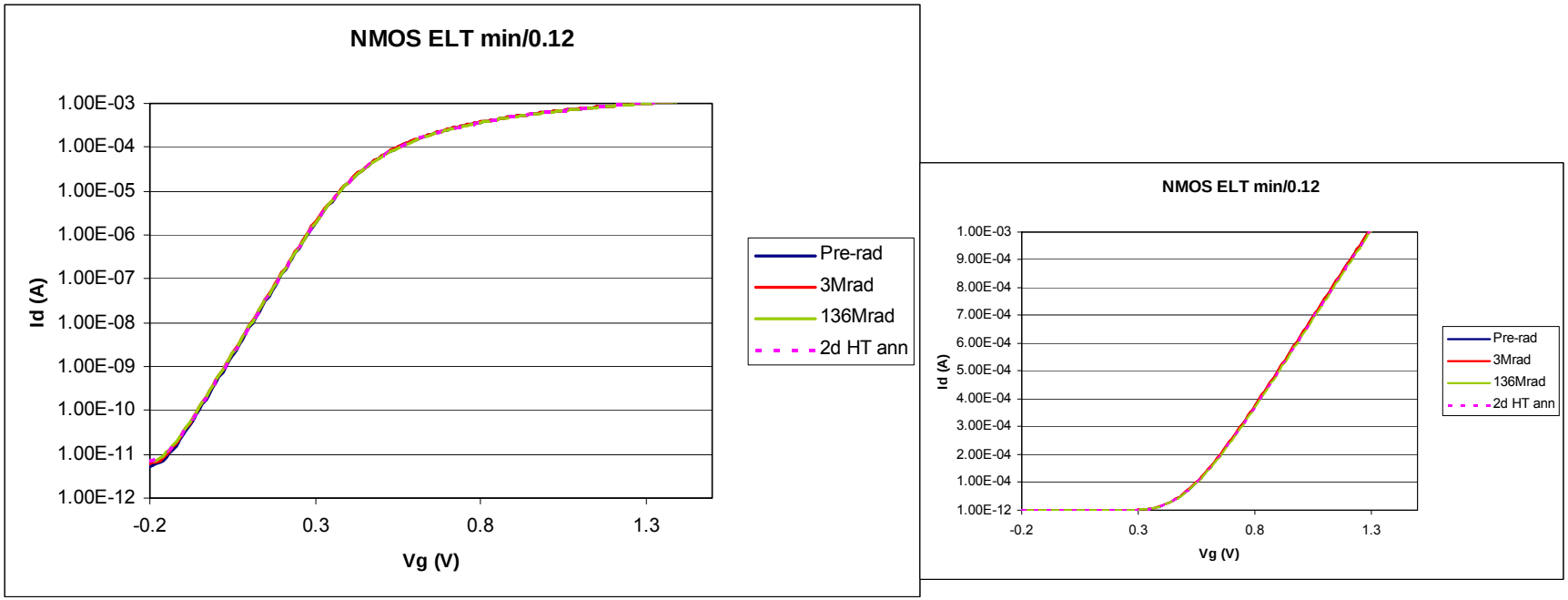




F. Faccio and G. Cervelli, "*Radiation-Induced Edge Effects in Deep Submicron CMOS Transistors*", IEEE TNS 2005

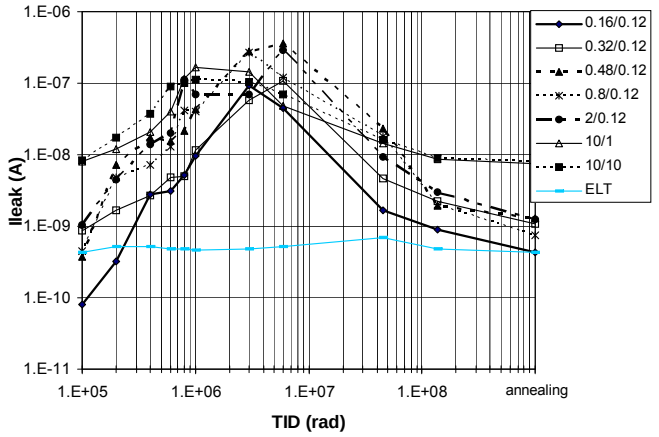
# 130 nm Core transistors, ELT layout

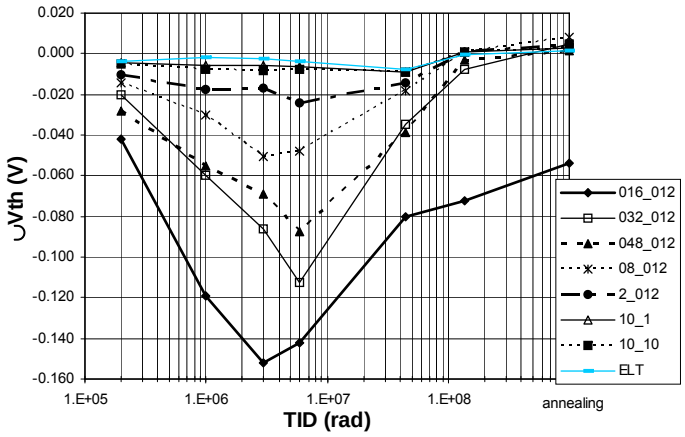
- The ‘natural’ radiation hardness of the gate oxide for 130 nm devices (in several fabs) is such that practically no effect is observed up to > 100 Mrad



# Core NMOS transistors, linear layout

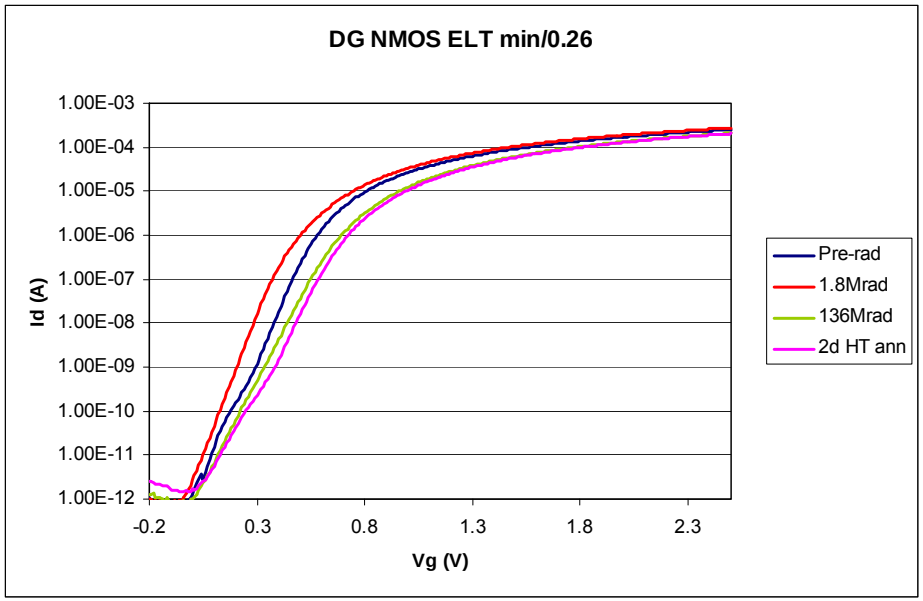
- Comparing with enclosed transistors, it appears that all effects on linear transistors are due to edge effects
- A “peak” damage dose exists, due to the antagonism between two different mechanisms (trapping in the oxide, and interface states)
- It is very difficult to forecast the behavior in a real dose rate environment, since interface states formation is difficult to characterize
- CAREFUL: annealing of charges for leakage is very slow! At doses of 1-10Mrad there will be leakage in the real application, for all widths!

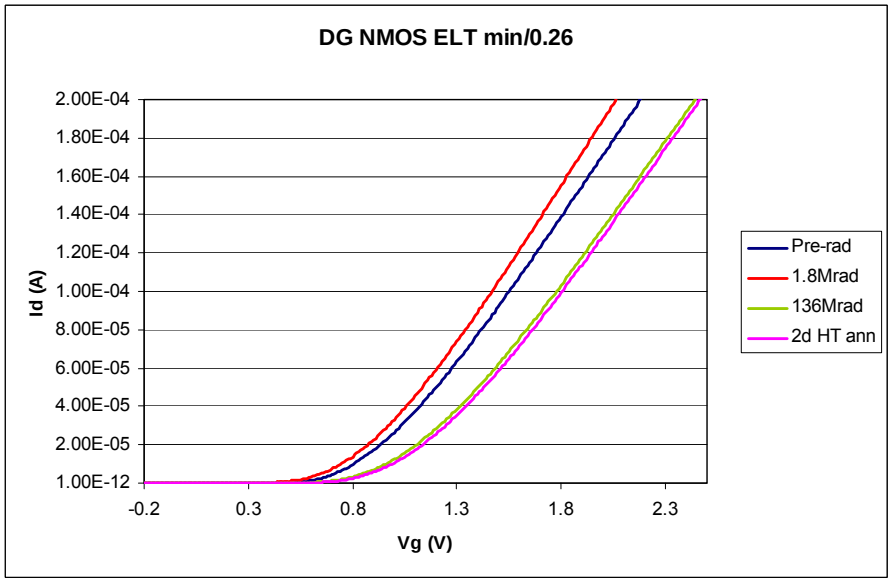


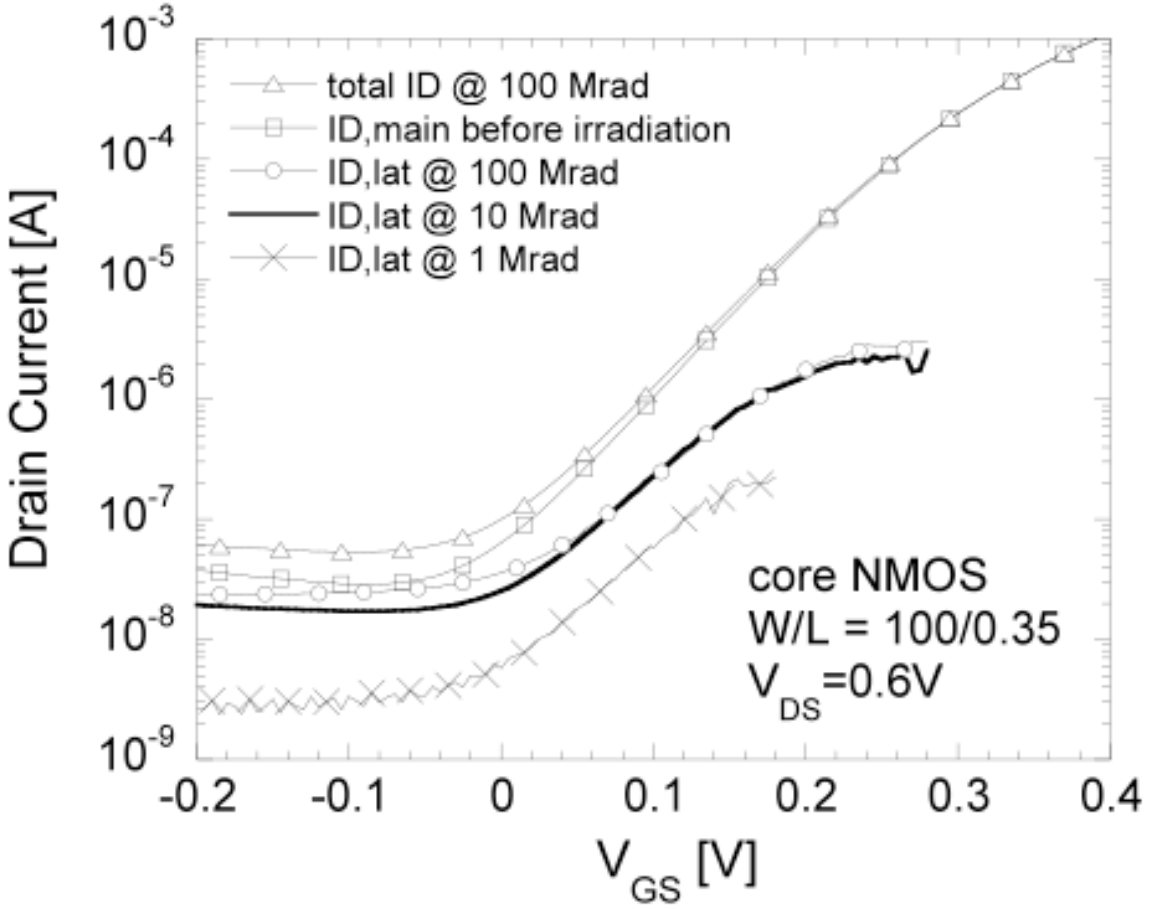
# IO NMOS enclosed transistors

- Due to the thicker gate oxide (≥ 5 nm), IO transistors need likely to be enclosed.
  - Unfortunately these may not be useable for “pure-analog” applications
  - But still perfectly OK for digital I/O
- A rebound is observable in the $V_{th}$ shift, showing the influence of both trapped charge and interface states



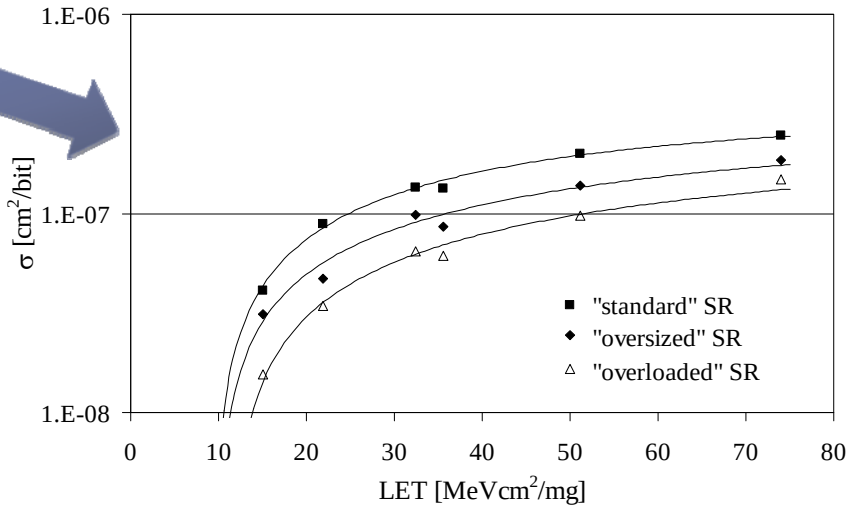
# 90 nm TID




Courtesy of V. Re et al., "*Comprehensive Study of Total Ionizing Dose Damage Mechanisms and their Effects on Noise Sources in a 90 nm CMOS Technology*", at NSREC 2008c

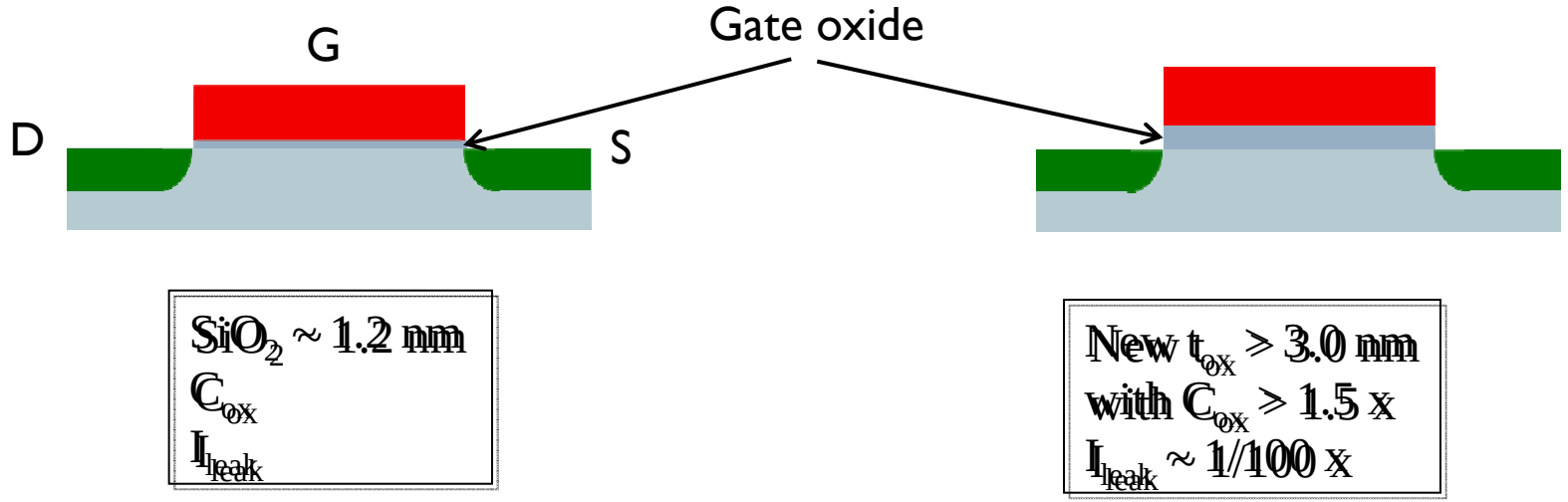
# Mitigating SEU

- Several techniques available and (well) understood
  - Increase cell area
  - Add cell capacitors
  - Introduce circuit redundancy
    - Many options available
      - Triple (space) redundancy
      - Double (time) redundancy
      - …
  - Error Correction Techniques




Upset rates in proton environment:
- twofold decrease for the “oversized”
- tenfold decrease for the “overloaded”

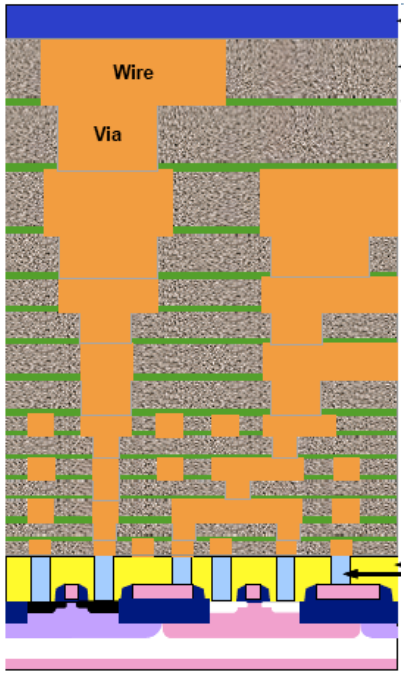
# Radiation and new gate dielectrics




- At $t_{ox} \leq 45$ nm new gate dielectrics are being introduced to eliminated tunneling through the gate
- These new compounds ($HfSiO_4$ and $ZrSiO_4$) have not yet been evaluated for radiation hardness

# Conclusion for radiation effects

- As long as we continue with $SiO_2$ gate oxides
  (i.e. $t_{ox}$ > 45 nm), no surprises are expected
  - Low-K dielectrics (used in interconnect isolation) should be investigated too
- Standard layout and ELT will cure TID problems
- SEU to be taken into account at circuit, logic and system levels
- No evidence for destructive SEL



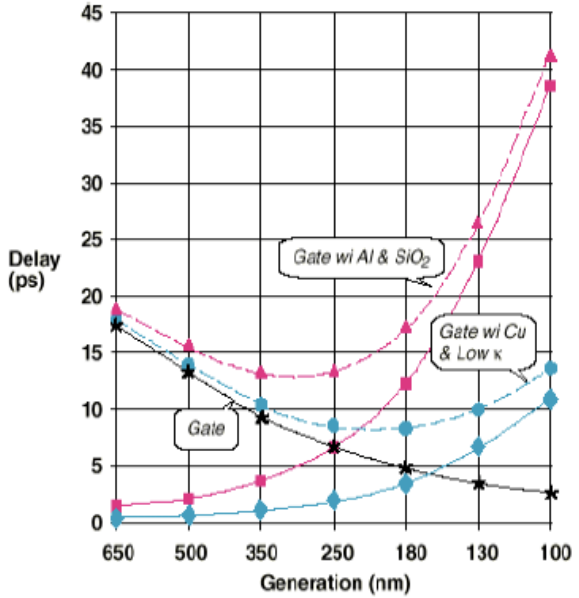
# Connectivity (local and global)

# Connectivity levels

- Chip-level connectivity
  - Scaling helps when deep submicron can be used
- Module-level connectivity (< 10-50 cm) is necessary for:
  - Connecting sensor to FE chip
  - Connection among FE chips (e.g. CMS tracker trigger primitives)
  - Connection to local data concentrators (“rod” or “stave” level)
- Long range (> 1 m) connectivity
  - Data concentrators to counting room
  - Monitoring, Control and timing (counting room to and from FE)

# Chip-level scaling

- Delay scales only if circuit size decreases




- Bottom line
  - In most applications, analog does not take much advantage of technology scaling
  - Digital does scale
    - Use more digital local processing
    - Do not move data, reduce it!

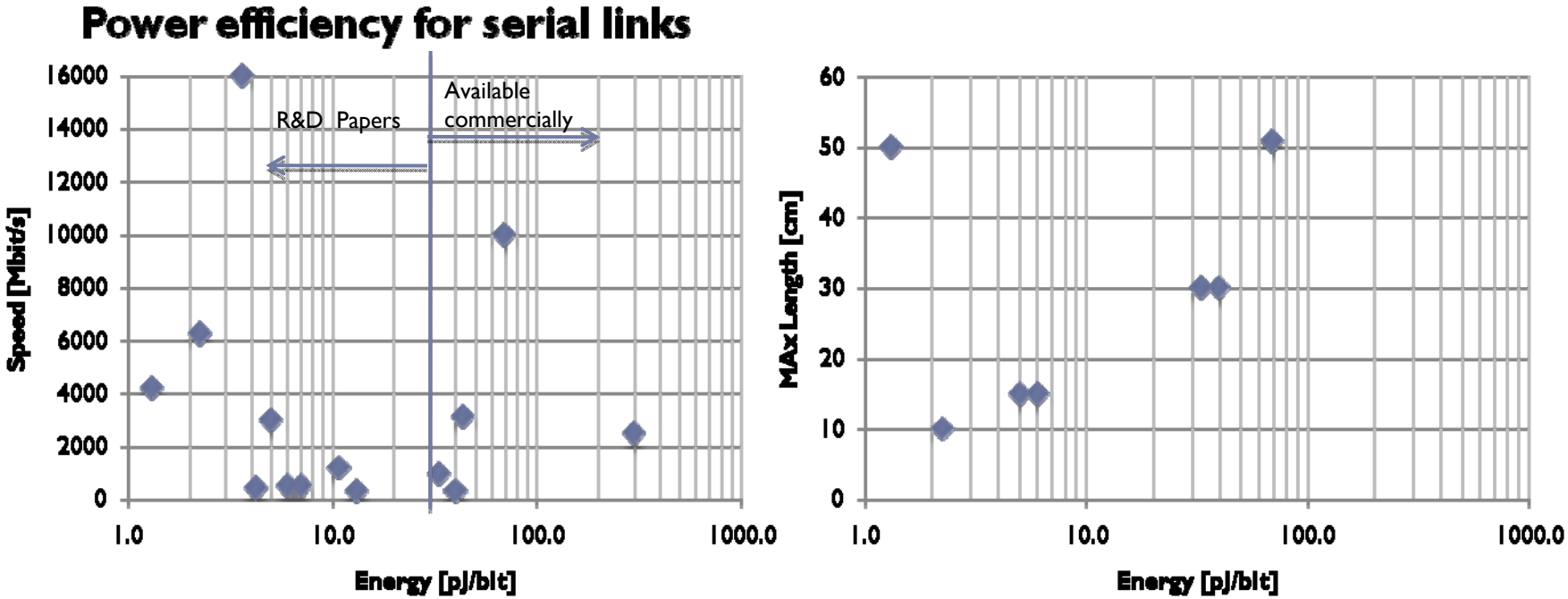
# Module-level connectivity

- Pixels
  - 3D(§) is very appealing, but can it be afforded?
- Trackers
  - Need low cost connectivity (and assembly) technology for channels ~ 0.1 mm x 10 mm
    - Many choices available
    - Need simplification of module and system assembly procedures
      - Too much manual work was required for module assembly in first LHC generation
- Everything else
  - No special needs ahead of well proved commercial solutions

§ Def: 3D is the stacking of multiple chips/sensors in direct contact (i.e. no bumps etc.)

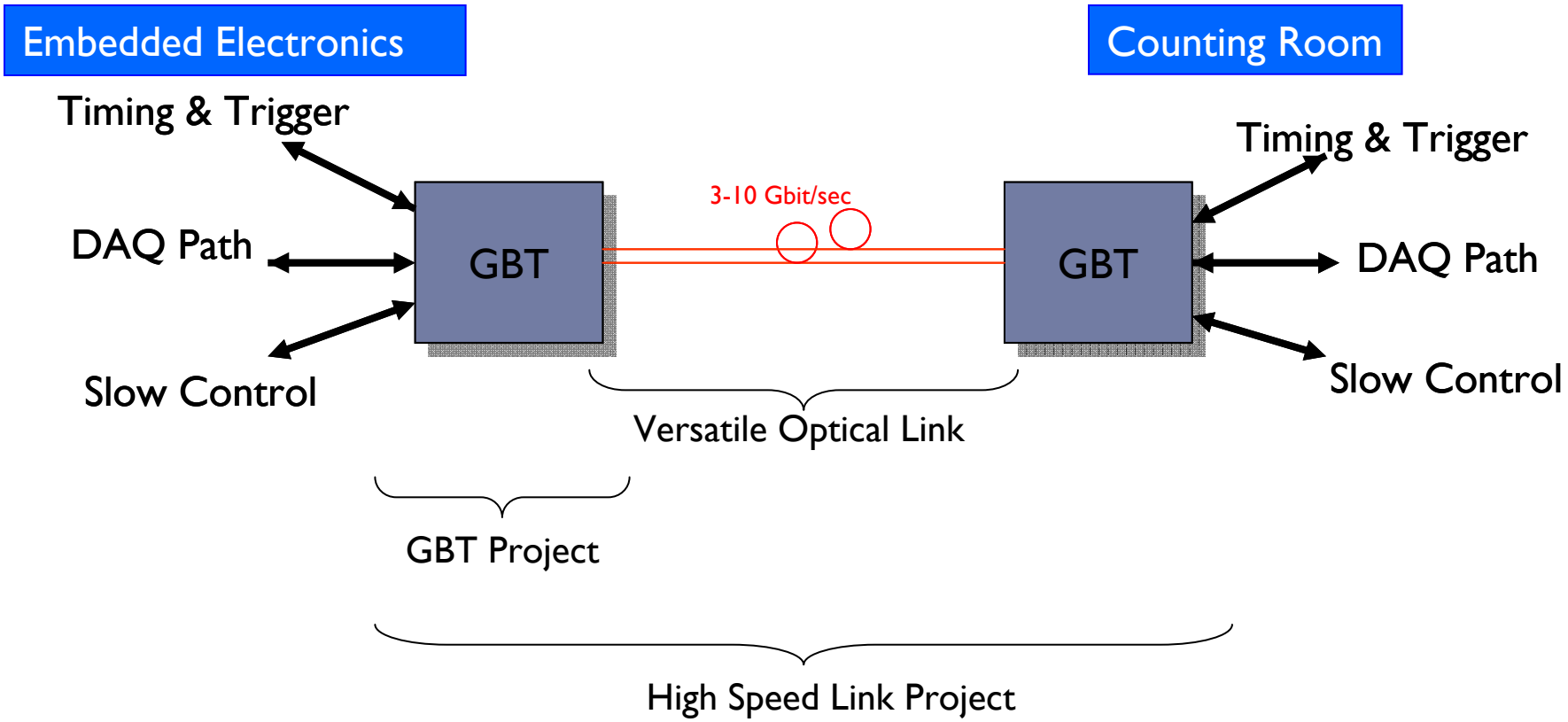
# Local connectivity

- Connectivity at the 1 to 20 mm level for trigger primitives
  - Issue: power

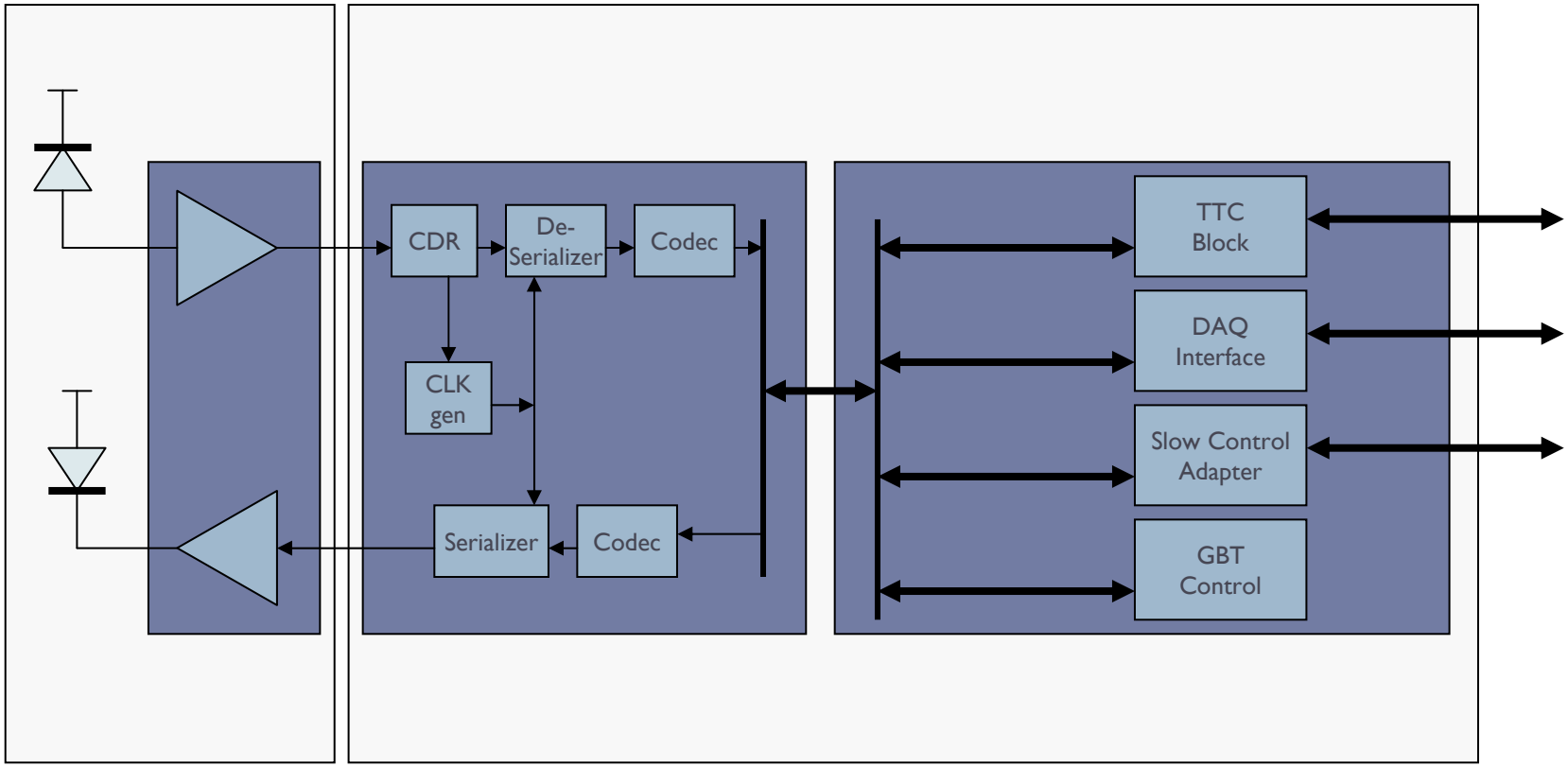


# Long range connectivity

- 10 Gbit/sec chip-sets at < 100 CHF/link appear feasible (*90 nm required*)



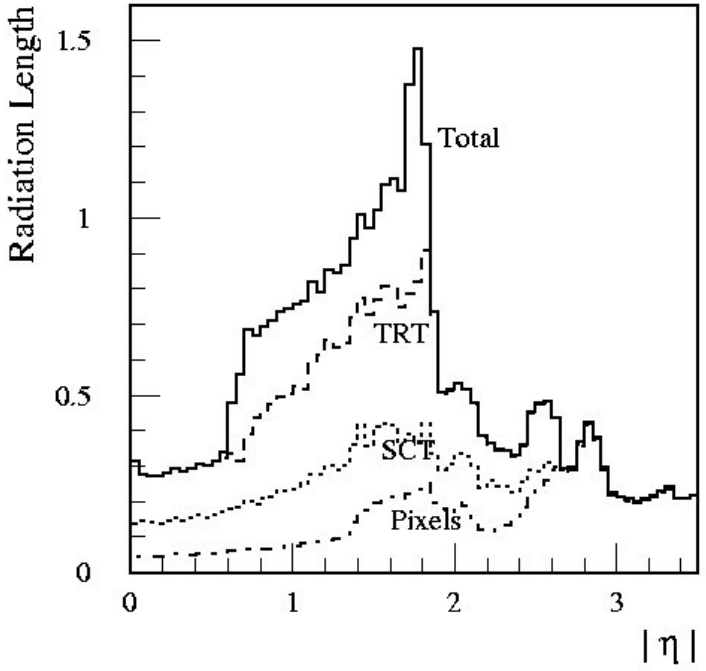
# Long range connectivity example: The GBT project



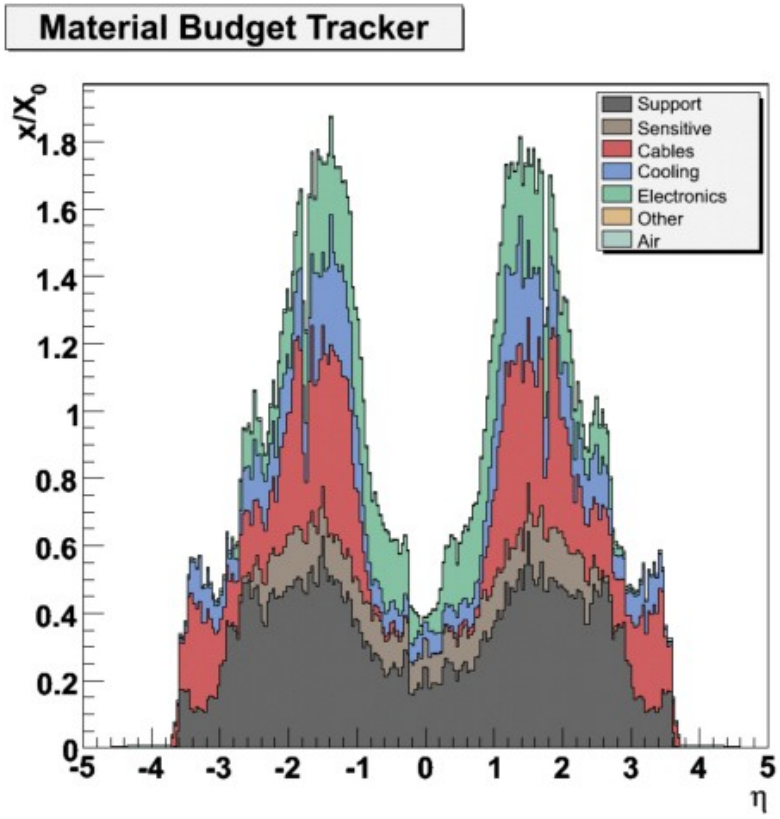

- GBT Functionality: fairly standard serializer architecture with enhancements:
  - Short latency (trigger constraints)
  - Robust protocol (SEU problem)
  - Sophisticated error correction (requires high integration, i.e. advanced technology)

# Power to the trackers

# Power and material budget




Atlas tracker material budget



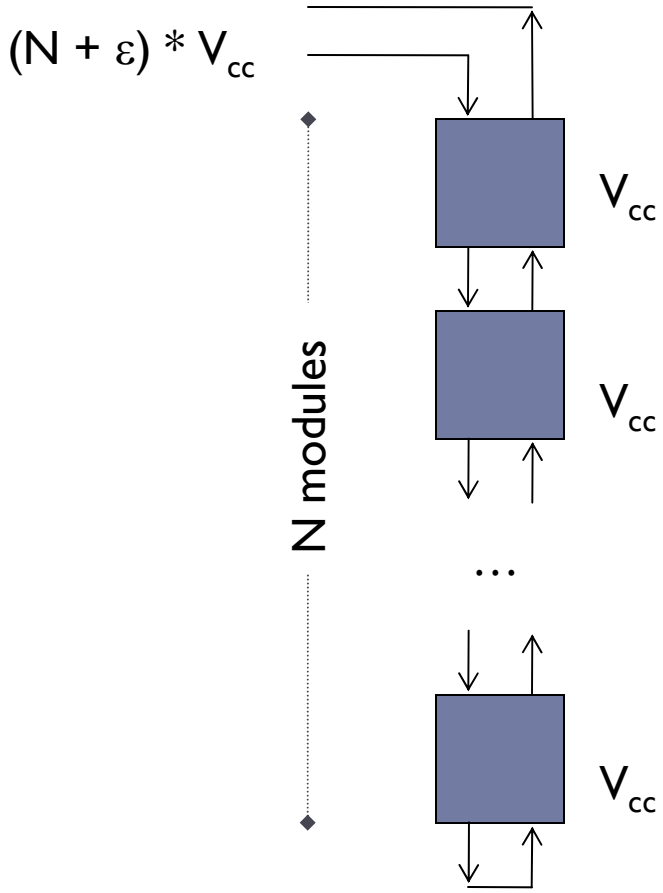

CMS tracker material budget

# Several levels of problems

- All other elements remaining the same, the material budget depends upon:
  - Total power actually used by the FE chips
  - Method of delivering the power to these chips
  - Method of removing the power dissipated

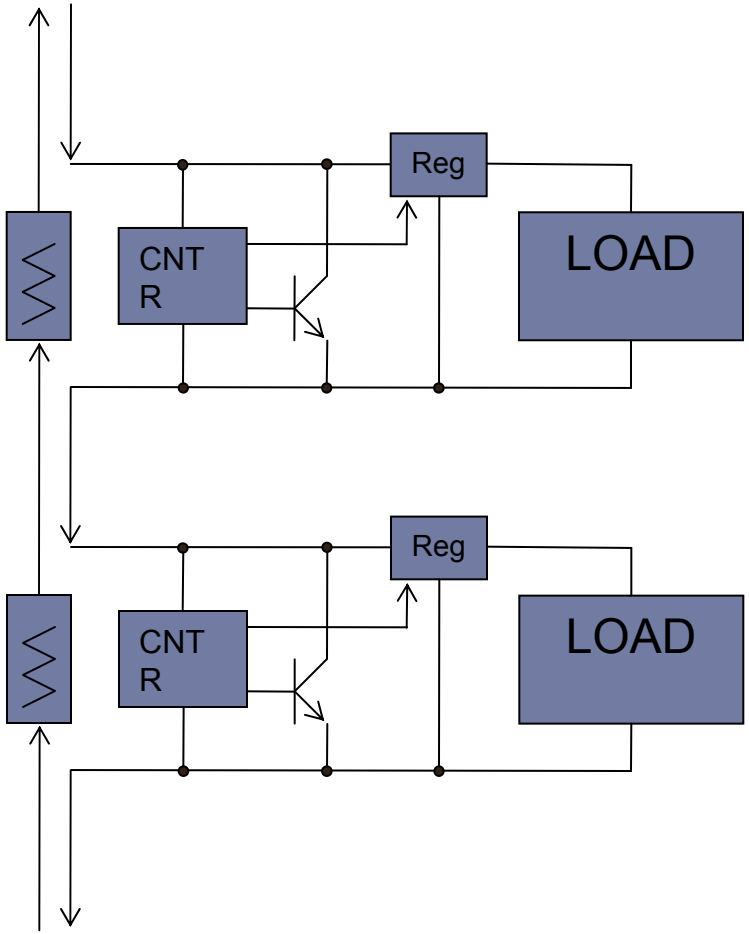
# Solution 1: Serial Powering

- Re-use the same current by assuming that current consumption is roughly similar in each module
- Main advantage: cables cross-section is divided by N



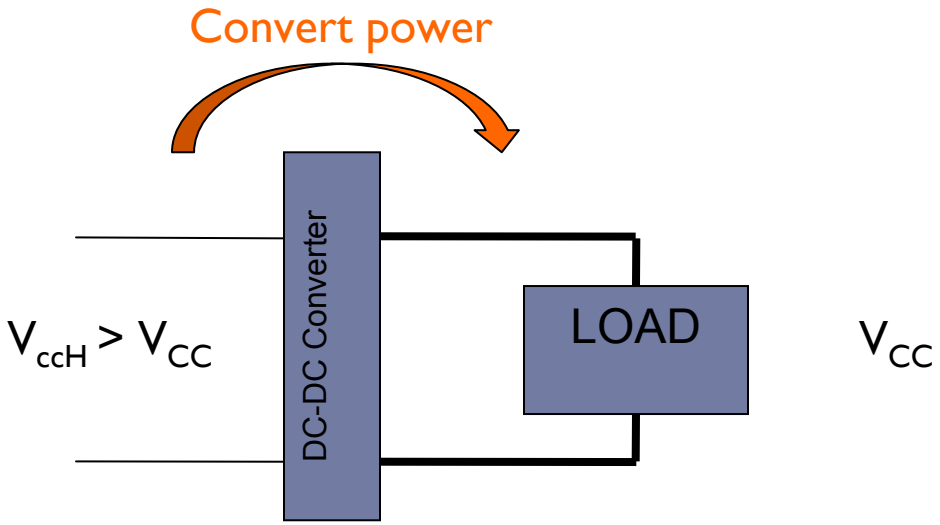
# Problems of Serial Powering

- Regulation performed by shunt device
- Some of the problems:
  - If load is turned-off, all current must go through the shunt
  - Stable regulation of a series of these objects is not trivial
  - No “ground” exist as reference: where do we refer the detector signal to, what about the sensor biasing voltage?
  - Links for data and control must be AC-coupled
  - Powering sequence is non-trivial
  - Whenever multiple voltages are necessary, these can be obtained only through (inefficient) linear regulators



# Solution 2: DC to DC down conversion

- Reduces cross section of cables up-to the converter




Ideal behavior: $I_H V_{ccH} = I_L V_{cc}$

Reality: $I_H V_{ccH} = I_L V_{cc} +$ losses

# Problems of DC-DC converters

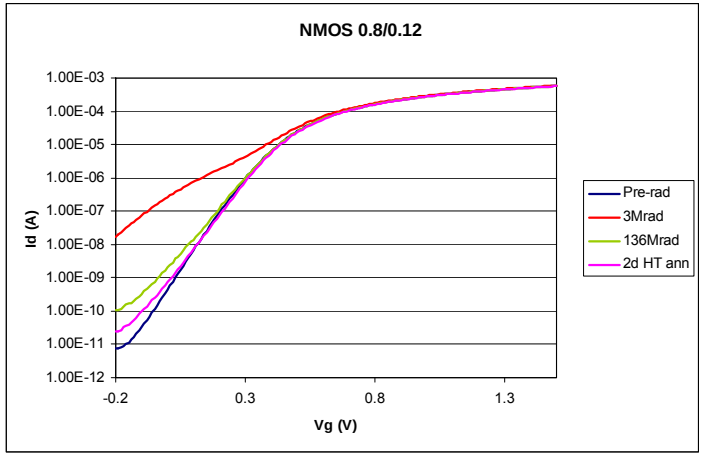
- Copper amount can not be optimized after converter
- Ratio $R=V_{CCH}/V_{CCL}$ can not be arbitrarily large
  - Maximum efficiency is reached with R about 10
- Due to high B-field in experiment, coil must be in air (potentially large)
- Noise produced by the switching on-off of the magnetic field storage must be avoided (shielded)
- Efficiency must be carefully optimized
- Rad-Hard power devices are needed

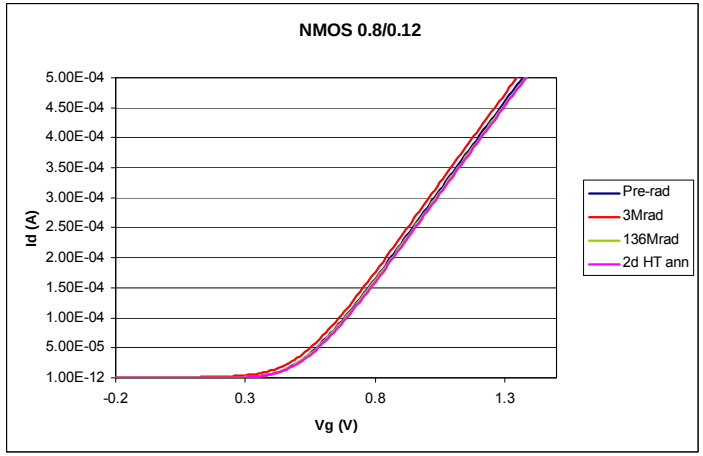
# Conclusions

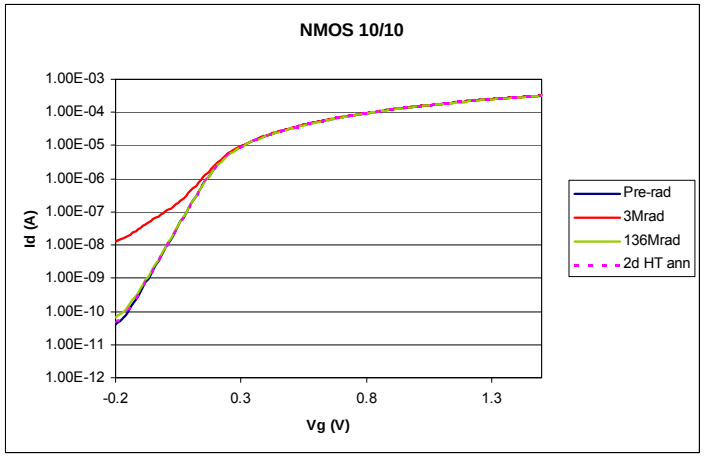
- Radiation problems:
  - No obvious showstopper in sight
    - DC/DC needs more work for HV devices
  - Rad Tolerant ASICs are feasible with proper organization among the designers
- Connectivity
  - 3D is very fashionable, but is it really necessary in large scale?
  - Substantial effort necessary to develop very low-power short-haul links
  - Long-haul links are feasible, but power optimization requires using advanced technologies, circuit techniques and aggressive signaling technologies
- Powering
  - Reducing the material budget of new trackers with 4-8 times the # of channels will be the most difficult SLHC problem

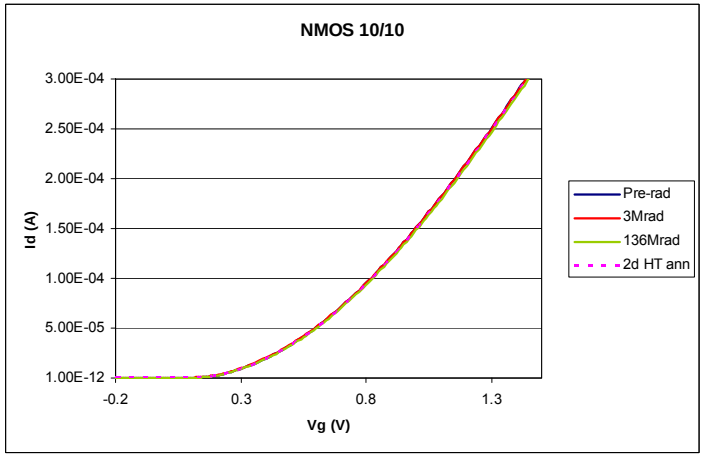
# Spare Slides

# Core NMOS transistors, linear layout (2)

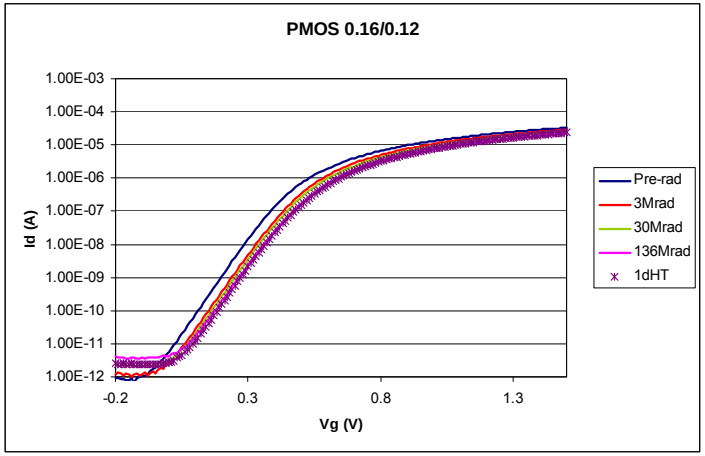


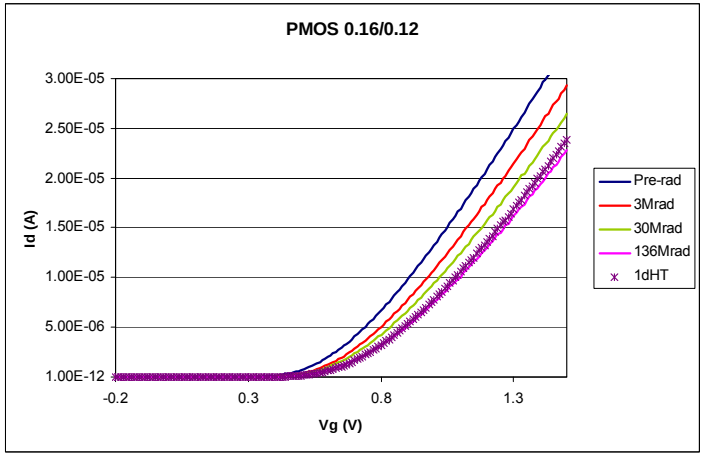



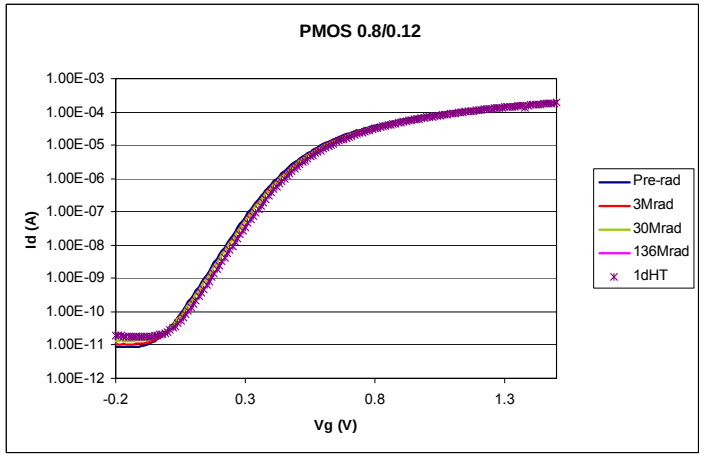



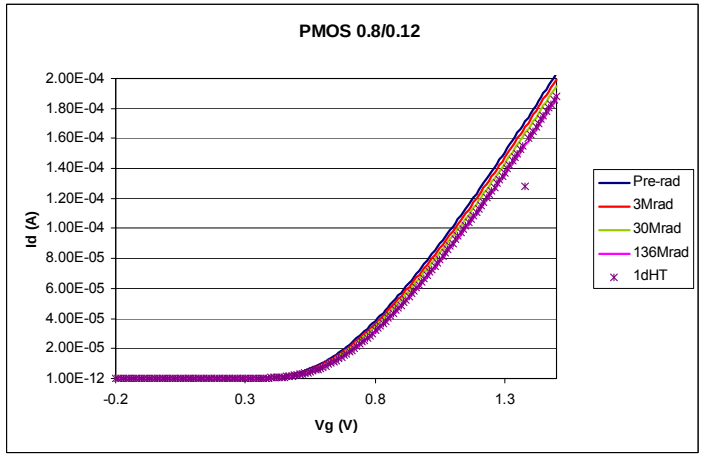



# Core PMOS transistors (1)

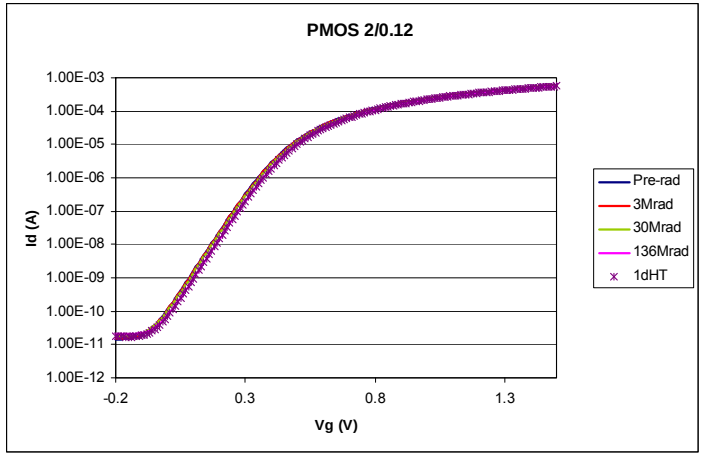


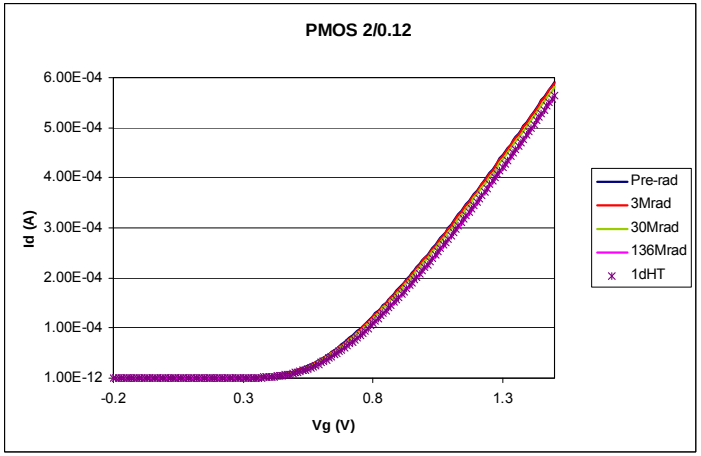



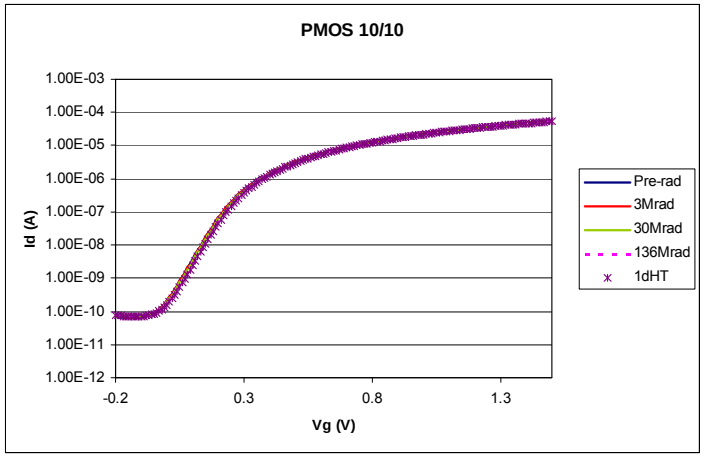



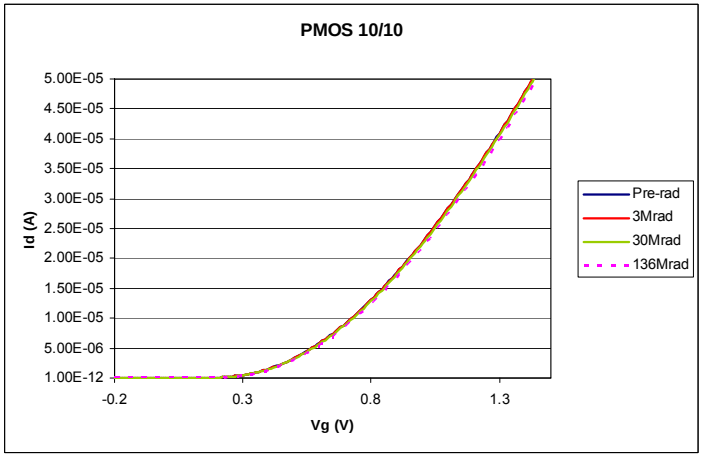



# Core PMOS transistors (2)



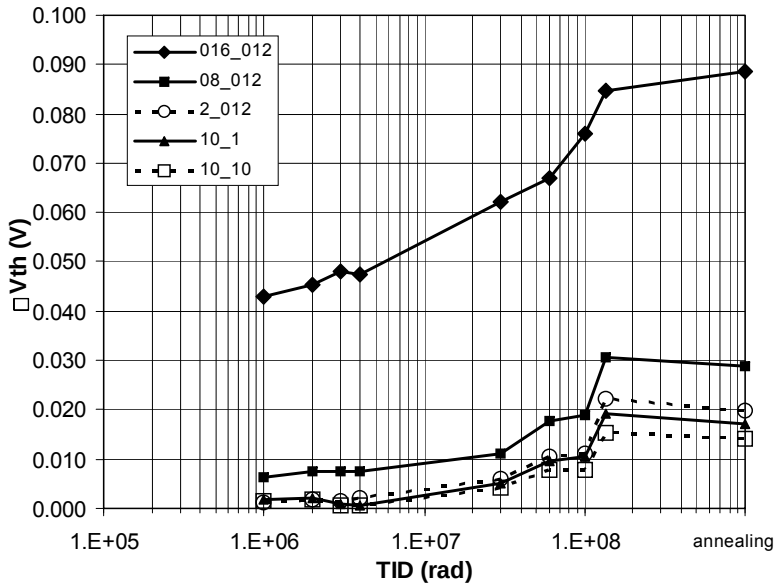



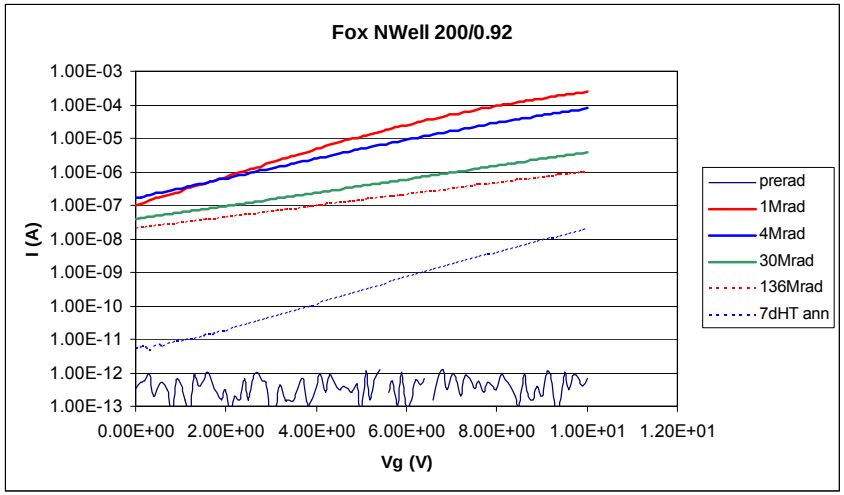
# Core PMOS transistors (3)

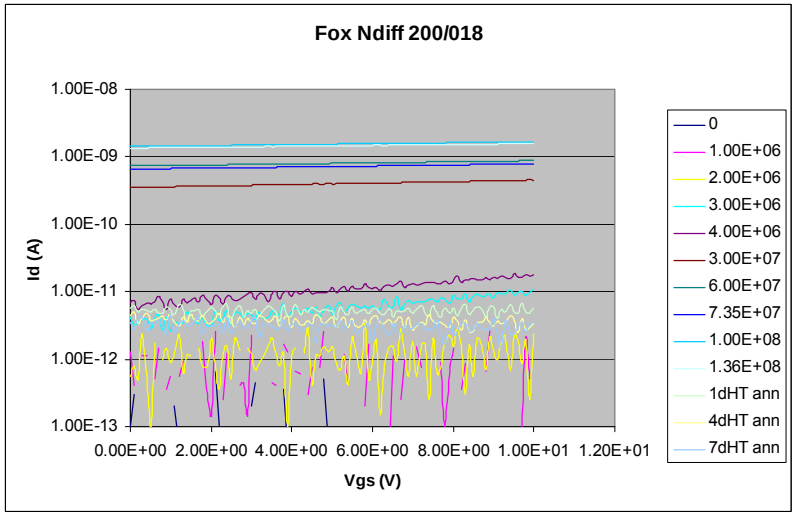
- Edge effects (trapped oxide charge and interface states) are not antagonist, but add up. Therefore there is no peak, but a continuous shift of Vth
- The effect is more pronounced for narrow transistors



# FOXFETs

- Also in this case, a « peak » can be distinguished (isolation oxide has similar properties to lateral oxide)
- Not a problem for digital (all wells at Vdd, low level of inter-transistor leakage), but care must be used for full custom to avoid large effects



# IO NMOS transistors, linear layout