N_{eff} tuning in MCz-Si detectors by isothermal annealing

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- ✓ Motivations
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- Conclusions

Aim of the work

Starting from the talk presented by J. Harkonen at 4th RD50 Workshop, May, CERN, systematically perform N_{eff} tuning to produce p⁺nn⁺ detectors on high resistivity Cz Si

- Process p⁺/p/n⁺ diodes from p-type MCz-Si few kWcm (Okmetic)
- 2. Activate shallow thermal donors via an isothermal annealing cycle
- 3. Measure at each annealing step the full depletion voltage and N_{eff} sign by Transient Charge Technique (TCT)
- 4. Evaluate TDs activation
- 5. Aim is modulation of N_{eff} by isothermal annealing to achieve easily high resistivity $p^+ n/p n^+$



Experimental

 \Box Six p⁺/p/n⁺ diodes (active area 0.25cm², thickness 300µm) manufactured on p-type Cz Si Okmetic wafers (nominal resistivity 5kΩcm) at the Helsinki University of Technology, Finland .

□ Devices studied at BNL by Transient Current Technique using a pulsed infrared laser (660nm) beam placed close either front or back electrodes. Collected charge measured in the range 0-400V, to determine full depletion voltage and sign of the effective space charge concentration N_{eff} .

□ An isothermal annealing cycle has been performed at 430°C with different time interval from 45min to 120min. TCT has been measured before and after each annealing step.

Results before annealing

As the devices are $p^+/p/n^+$, when the reverse bias is increased the space charge region develops from the back electrode. The signal is measured with laser front only when $V_{rev} \ge V_{fd}$, while it is always measured from back if $V_{rev} \ne 0$



Signal integrated in time, plotted against Vrev to determine the $\mathrm{N}_{\mathrm{eff}}$ sign



Sample	V _{fd} [V]	N _{eff} [10 ¹² cm ⁻³]
P7	262,00	- 3.86
P8	226,65	- 3.34
P17	229,05	- 3.37
P46	232,95	- 3.43
P57	237,15	- 3.49
P58	214,75	- 3.16

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No correlation between N_{eff} and position in wafer



The TCT measurements are repeated for each diode after 5 different annealing steps (0-45-65-90-120min) at 430°C. Samples invert from p to n-type in between the two last annealing steps.



Annealing activates TDs which compensate the shallow Boron present in the starting material: very high resistivity, up to **r** ~10-30kWcm, are achieved.



At the last annealing step a N_{eff} with positive sign is measured for the 6 diodes. The depletion region moved to front electrode.



Full depletion voltage as measured with TCT



The generation rate for N_{eff} is not correlated to the initial N_{eff} value, but depend on the position of the diode inside the wafer $\rightarrow O_i$ concentration or other impurity involved





Initial N_{eff} (\Box)/ N_{eff} (\Box) = 1.05 Final N_{eff} (\Box)/ N_{eff} (\Box) = 2.8

In the simple hypothesis:

$$N_{eff} = N_{eff}(0) + b(T)^* t$$

b = (3.48 ± 0.30) x 10^{10} cm⁻³/min b = (4.61 ± 0.25) x 10^{10} cm⁻³/min

Conclusions

Changes of N_{eff} have been studied after up to 120min isothermal annealing with T = 430C on detectors processed on p-type Cz Si.

The procedure allows a fine tuning of N_{eff} to obtain high resistivity n- and p-type material.

Uncertainties in the procedure are given by fluctuations on the concentration of native defects (O_i , H, ...) locally affecting the generation rates. Starting with $V_{fd} = 220-260V$, final full depletion voltage varied in the range 50-150V.

DLTS studies of shallow thermal donors are planned on the treated diodes to study activation processes and wafer disuniformities.