Pixel Devices on the common RD50 Strip Detector Mask Set

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5th RD50 workshop, October 14-16, 2004, Firenze

Basic Considerations

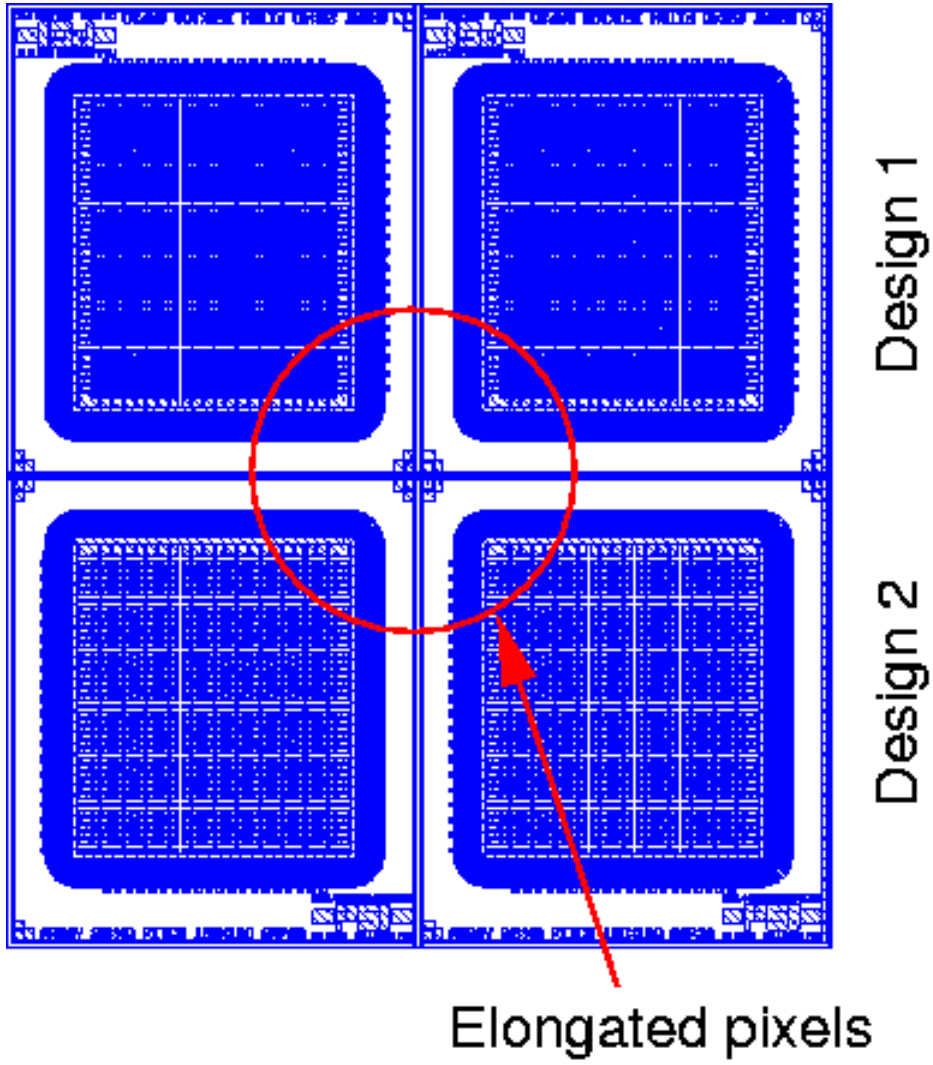
- "n-in-p" pixel sensors very attractive for sLHC
  - Single sided process (much cheaper than "n-in-n")
  - Potentially the same radiation hardness
- Mask set dedicated to "n-in-p" strip detectors
  - Process contains a poly layer
  - Contacts only possible via poly
  - No passivation
  - Process is double sided
- Pixel devices are "parasitic"
  - Cover only a small fraction of the wafer
  - Have to use the technology chosen for the strips

Implications on Pixels

- Design is derived from CMS barrel-pixel sensors but
  - Minimum feature size is larger
    - Bias structure different
    - Guard ring design different
  - Technology is slightly different
- Probably no Bump deposition on wafer level
  - Limits possible bump vendors
  - Expensive
  - Small number of devices (therefore no Problem)
- Poly cannot be avoided (contacts)
  - Is used as field plate (in the pixels and guard rings)
- Backside is unstructured
  - “n-in-p” technology should be single sided
  - No laser tests possible (probably a mistake ?)

Geometry

- Pixel size : $100 \times 150 \mu m^2$ (CMS)
- Array size: 22×40
  - Fits to a special ROC currently under design at PSI
- Sensitive area: $3.6 \times 4.1\ mm^2$
- Chip size: $5.4 \times 6.2 mm^2$
- 4 sensors next to each other, recticle size: $10.8 \times 12.4 mm^2$ (Fits into $12.5 \times 12.5 mm^2$)



Device Corner

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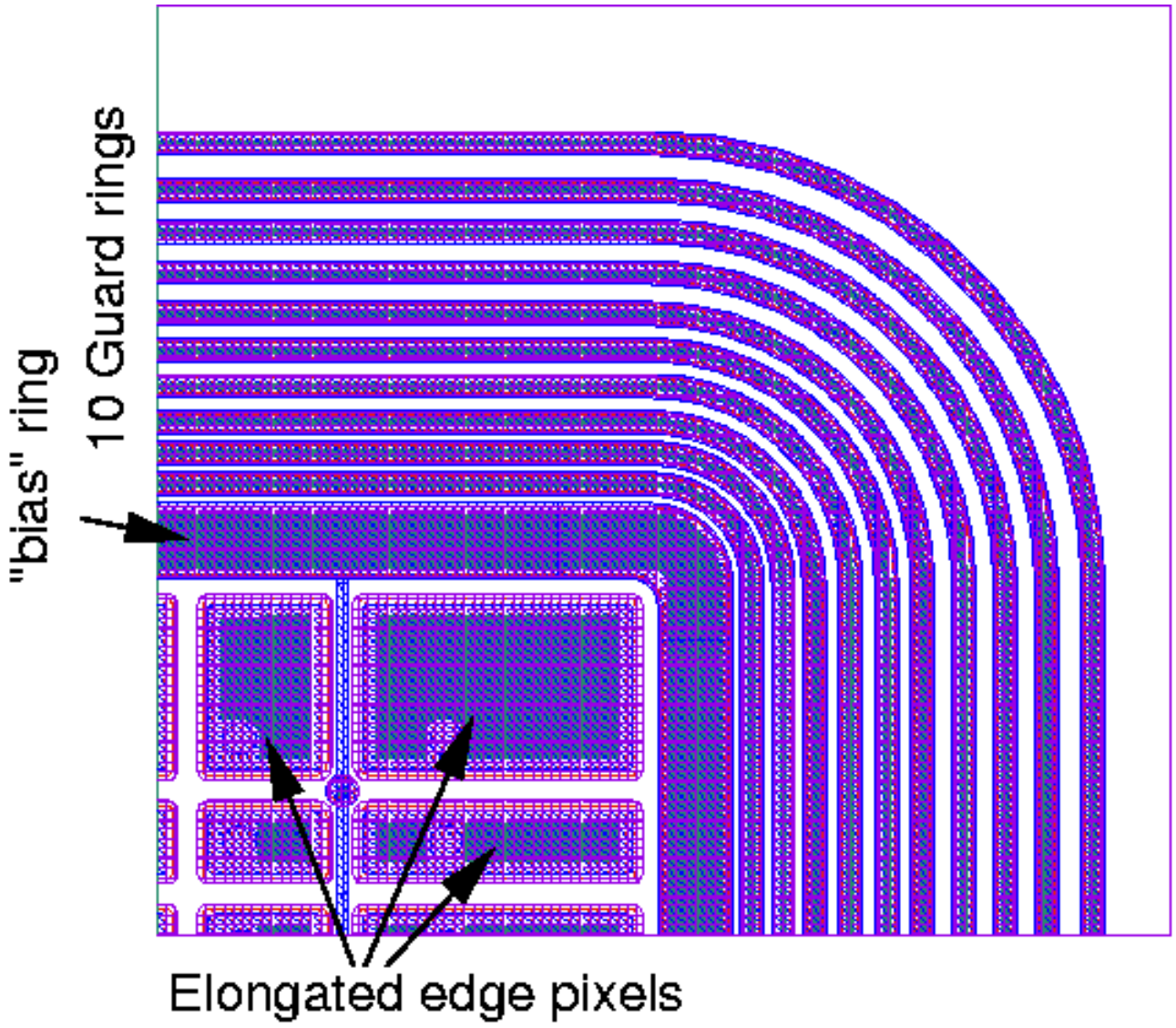
- Multi guard structure
  - 10 rings
  - Increasing gap
  - Overlaps in metal and poly
- Elongated edge pixel (for multichip modules)
- Distance sensitive area to scribe ~0.9mm



Pixel Design 1

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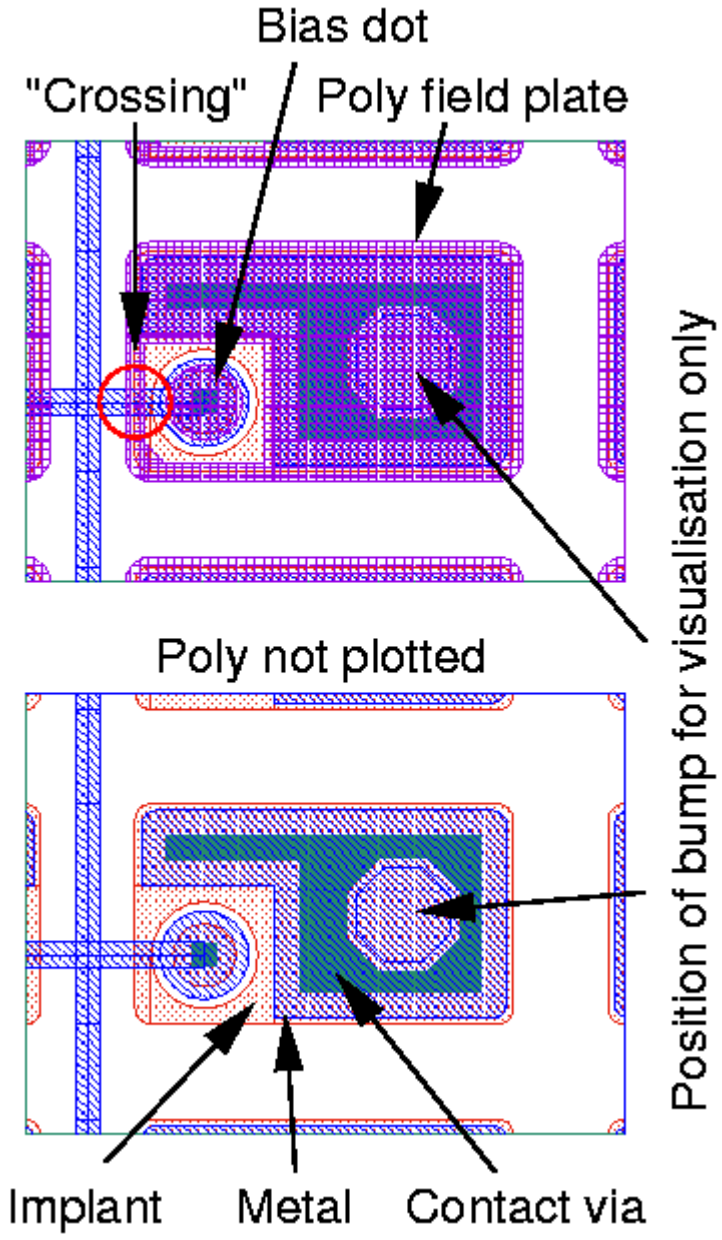
- As close to the ATLAS/CMS-barrel design as possible
  - Gaps larger
- Bias dot
  - Testability
  - Small area affected
- Poly used as field plate



Pixel Design 2

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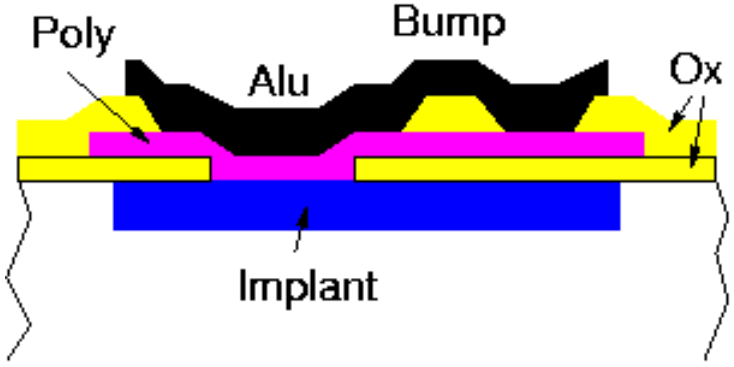
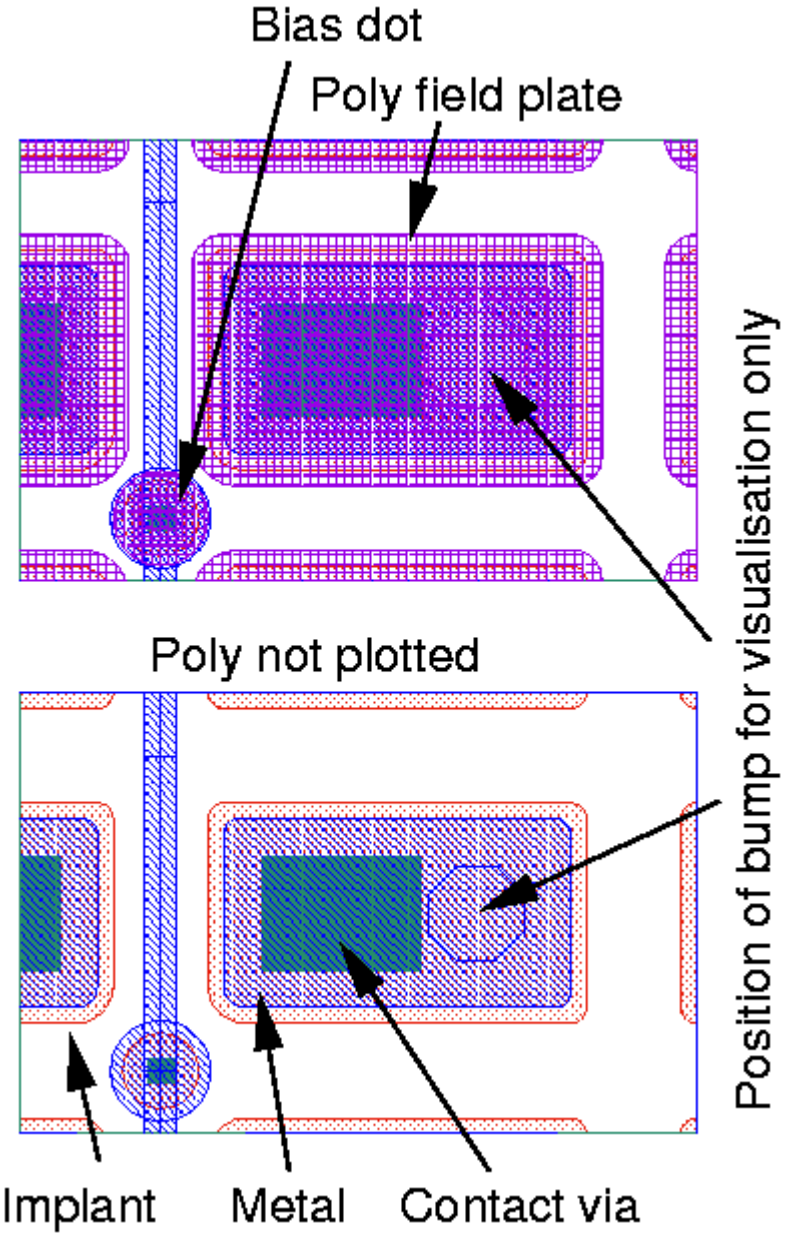
- As simple as possible
- Avoid features which might reduce the yield
  - Small distance “inner” bias dot
  - Crossing of metal and poly
- Signal loss due to bias structure more severe ?





Conclusions

- “n-in-p” pixel sensors submitted with strips
- Design close to such used in LHC experiments
- Poly of “strip” technology allowed/required the implementation of field plates
  - Potentially higher breakdown voltage
  - Not standard for DC-coupled pixel
  - 2 extra mask layers (costs)
- Sensors fit the analogue pixel readout chip currently under development at PSI

A Pixel Readout Chip for Sensor Characterisation

R. Horisberger and T. Rohe
PSI

Motivation

Preliminary Specifications

Schedule

Motivation

- Sensor R&D for the CMS Pixel Barrel was done with a Honeywell-Version of PSI30 produced in 1997

  Important features:

  – **Full analogue readout without zero suppression possible**

  – Easy to operate

  But:

  – Not available anymore

  – Not sufficiently radiation hard (very painful bump bonding procedure of irradiated sensors)

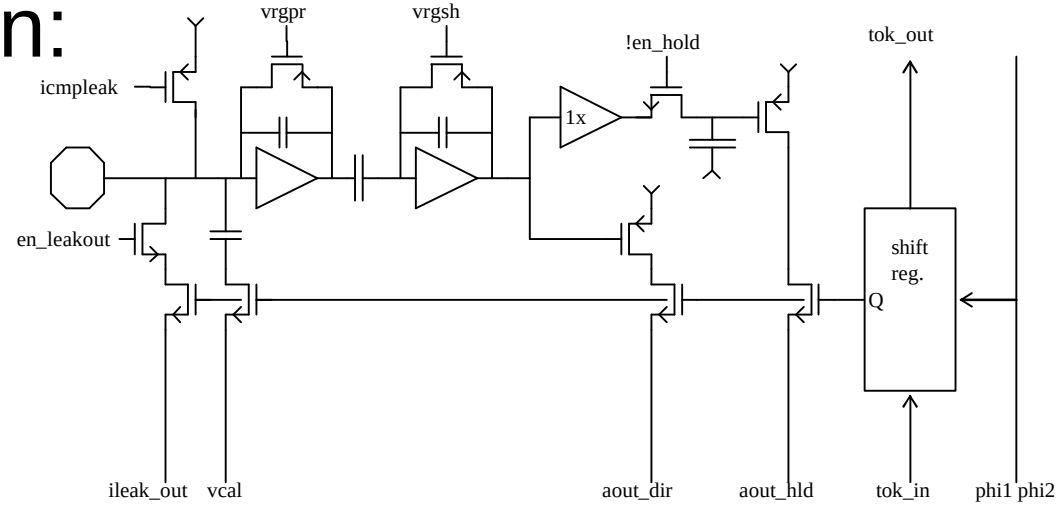
- Successor Chip needed

Boundary Conditions

- Has to be simple
  - Only 1-2 persons available
  - Not a “top priority project” for those
  - Readout system should be simple and inexpensive
- Close to CMS (otherwise it will be hard to allocate the personal resources and money)
  - Pitch of CMS pixels is ($100 \times 150 \mu m^2$) used
  - Analogue part of the CMS ROC is taken with minor modifications only (5 metal layers reduced to 3)

Basic Functionality

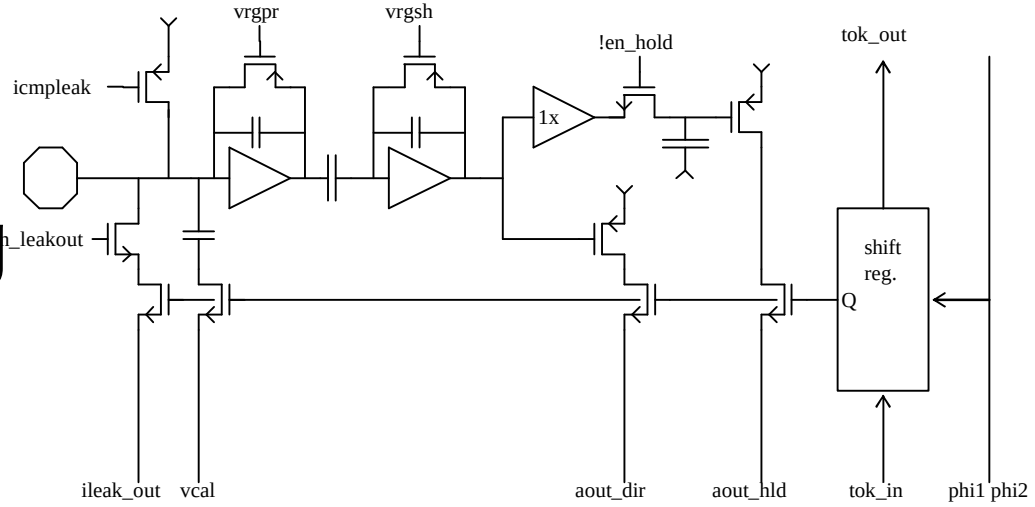
- No zero suppression:
  - No comparator
  - No trimming
  - No programming



- If external trigger (e.g. from back side signal) comes within 50-60ns to en_hold, analogue amplitude is stored on capacitor
- For readout
  - Token is clocked through a static shift register running along all cells.
  - Signal is available on aout_hld when token is in the cell

Additional Featues

- Token shift register can be used for simple programming
  - Inject calibration pulses Vcal into a capacitor (~8 fF)
  - Connect the shaper output to an external pin
  - Connect pixel leakage current to an external pin



- No of pins: 18
- Supply voltage: 2.5V (D) and ~1.2V (A)

Geometry

- Pixel Size: 100×150μm²
- Array 40×22
- Chip: 6 × ~3.5 mm²
- No of pins: 18, pitch 180μm
- Supply voltage: 2.5V (D) and ~1.2V, <10mA (A)

Status

- Circuit/Schematic: ready
- Layout: In progress
- Expected submission: MPW via CERN in Dec 04 ???? (has been delayed already several times …)
- Quantities: MPW = few chips, diced
- If chip good, interest and founding ok, purchase un-diced MPWs? (Engineering run too expensive > 100kCHF)