Development of Radiation-hard Front Electronics for sLHC

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Investigation of the SiGe Process

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Synergy of detectors and readout electronics.

"Detectors and Electronics: *Are These Two Separate Subjects?*"

(V. Radeka, 2003 IEEE NSS Portland, OR)

or:

When RD50 finds the ultimate radiation-hard detector material, surviving fluences in excess of 10^{16} n/cm^2 and TID of 300MRad, can we extract the signals?

F.E. Technologies for sLHC:

Sub-μm CMOS: “accidentally” rad-hard, low power, ideal for pixels

Bipolar : power-noise advantages for large capacitances and fast shaping, also excellent matching, used in ATLAS SCT

BiCMOS bipolar for analog front-end, CMOS for digital logic

BUT:

Silicon technologies show current gain β degrading with radiation,

for LHC from about 100 to about 40 at 10^{14}cm^{-2}

Present Si bipolar technologies are not rad-hard enough for sLHC.

It has been a struggle to have access with them, especially in proto-typing.

Enter SiGe

Epitaxial technology

Very fast: f_T of 50GHz and up,

Very high current gain $\beta > 200$

Rad hard: but how hard is "rad-hard" (measured up to $10^{14}cm^{-2}$)

(advantage: start out with higher β and FT)

married to sub-μm CMOS to make rad-hard BiCMOS

Driven by communications industry: is here to stay

Offered by MOSIS for manufacturing at IBM

Case study of advantages of SiGe Bipolar vs. CMOS

Power required for a front-end amplifier designed with a 20ns shaping time (ATLAS SCT) using the two technologies, SiGe bipolar and 0.25 μm CMOS.

The SiGe version is shown to require about 1/3 of the power of the CMOS version for the same noise performance.

For shorter shaping times, the advantage would become even more pronounced. For certain radiation hard detectors, such as diamond, shaping times under 10 ns are optimal; and for some potential applications, as an upgraded LHC, shaping times of 10-12 ns may be necessary.

The technology, therefore, appears to be extremely promising, provided that it is sufficiently radiation resistant.

Power of SiGe Bipolar vs. CMOS

CHIP TECHNOLOGY **FEATURE**	0.25 μm CMOS ABCDS/FE (Jan Kaplon et al., 2002)		IBM 7HP SiGe (Ned Spencer et al.)	
Power: Bias for all but front transistor	400 μA	1 mW	80 μA	0.2 mW
Power: Front bias for 25 pF load (Total power)	550 μA	1.38 mW (2.4 mW)	195 μA	.49 mW (0.69 mW)
Power: Front bias for 7 pF load (Total power)	120 μA	0.3 mW (1.3 mW)	60 μA	0.15 mW (0.35 mW)
Channel-to-channel matching at comparator	+/- 6%		+/- 4%	
Band gap reference available with radiation resistance	Probably not		Yes	
Noise for 24pF load	1480		1360	

Why Faster Shaping?

At 40 MHz LHC operation, and charge collection times of about 20ns, the 20ns shaping time of the ATLAS SCT makes sense to tag single beam buckets.

BUT: for sLHC, the machine frequency will be doubled.
ALSO: For LC, interest to tag out-of-time tracks from γ–γ

So investigate if SSD can be operated with 100MHz clock, without ballistic deficit and acceptable noise penalty.

Increase SSD biasing voltage (decrease collection time τ_C)
decrease shaping time τ_S
(Bruce Schumm, John Jaros)

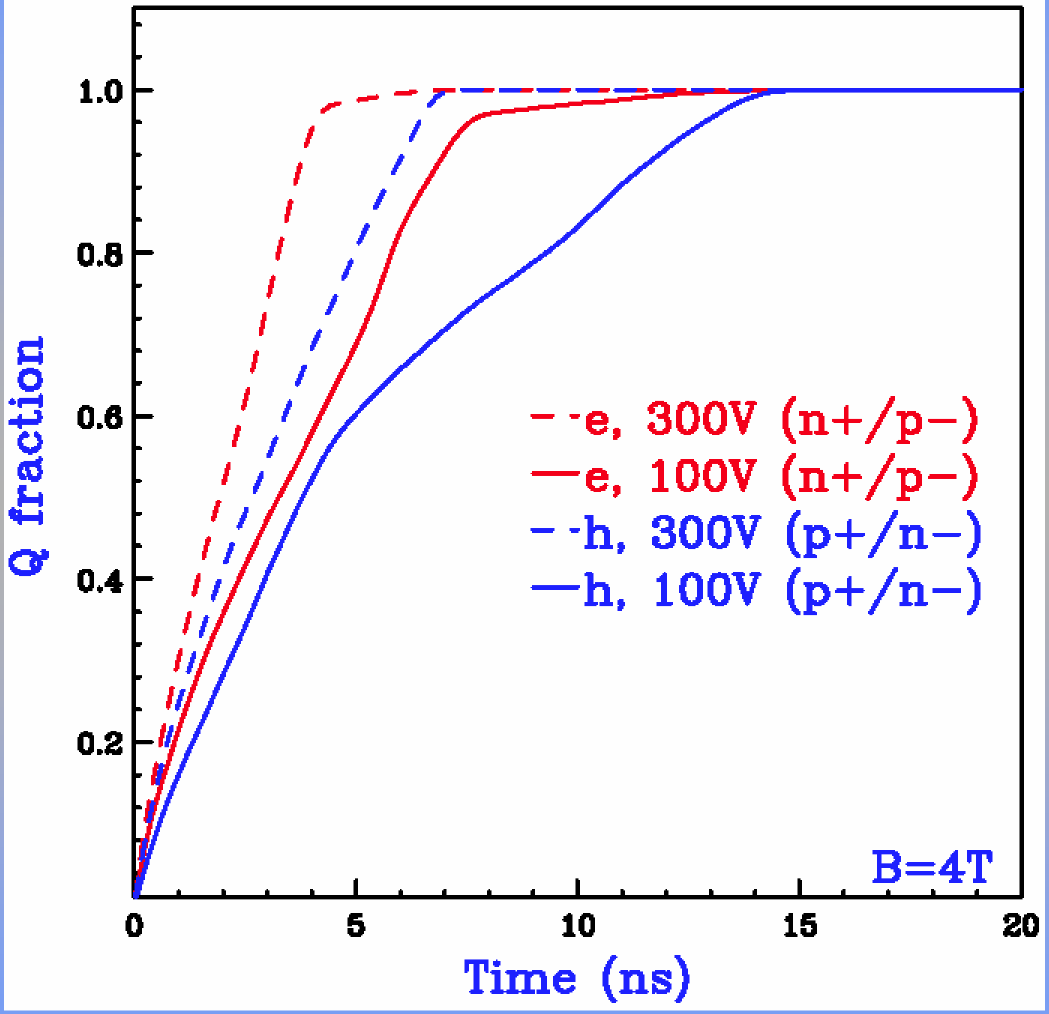
Charge Collection in Si

(thanks to Morris Swartz, JHU)

300um thickness,
50um pitch
60V depletion voltage

p-on-n	Collection Time [ns] 100V	300V
Holes	14	7
Electrons	5	2.5

N-on-p factor two faster.

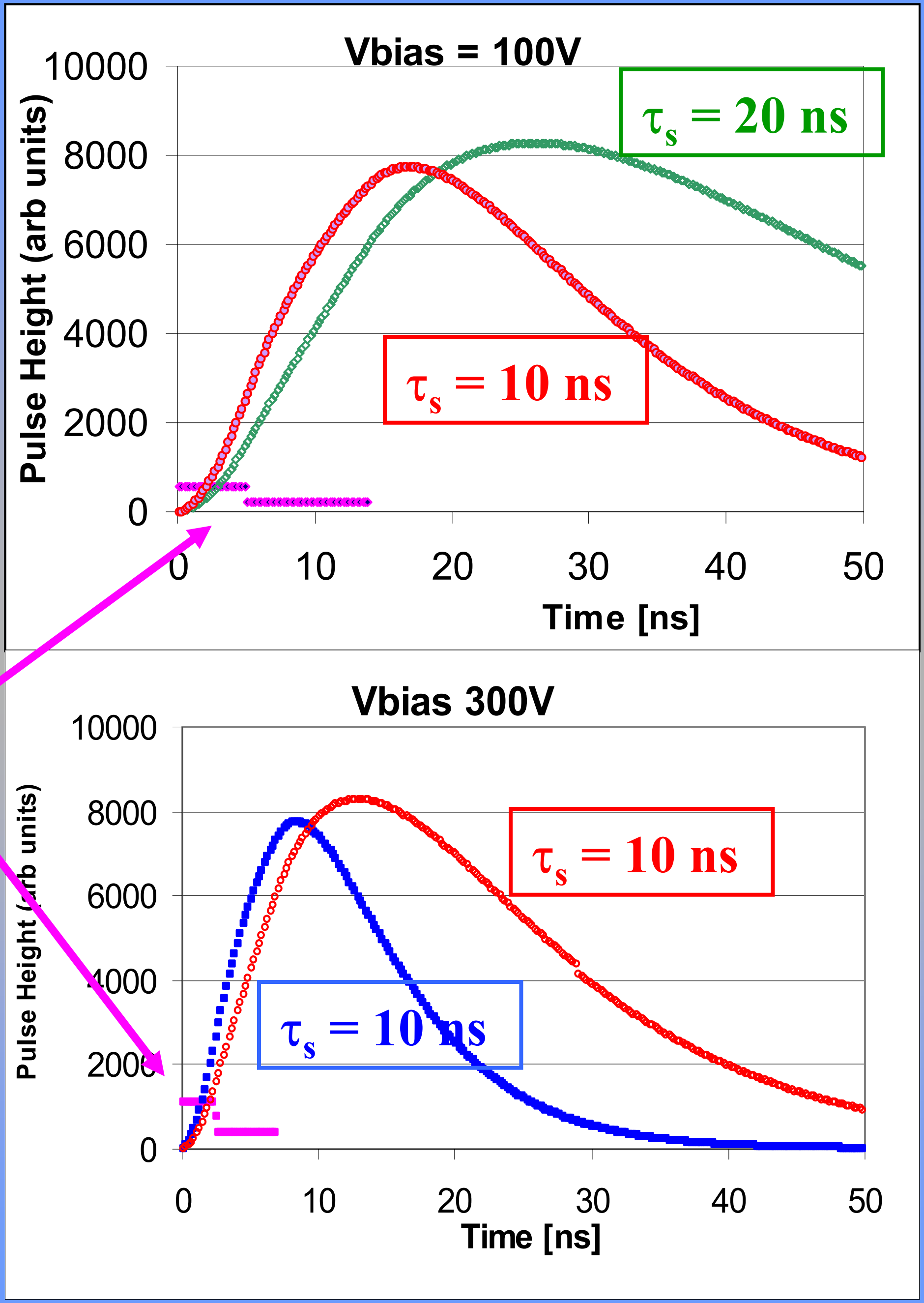


Time-tagging
vs.
Shaping time:

Vbias = 100V
τ_s = 20 ns, 10 ns

Approximate current pulse

Vbias = 300V
τ_s = 10 ns, 5 ns



10 ns shaping and 300V bias allows 100Mhz time tagging.

SiGe R&D Program

(to US DoE Advanced Detector Research Program)

Collaboration with John Cressler's group at the Georgia Institute of Technology

Year 1: Spice simulation of amplifier circuits,

Design and fabrication of test structures and simple circuit elements

Test matching, radiation hardness {including degradation of β and noise increase} and other parameters.

Year 2: Design and fabrication of a front-end ASIC for readout of silicon strip detectors and thorough characterization.

Compare the SiGe performance to other options.

Year 3: Perform radiation tests to understand the limits of the technology.

Integrate with silicon strip detectors and evaluate noise performance.

In Partial Fulfillment of the Requirements for RD50 Membership:

The Group:

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Interests:

- Development of Radiation-hard Front Electronics for sLHC (SiGe)
- n-on-p detectors
- 3-D detectors
- System Aspects

Front-end ASIC Development to which SCIPP has contributed

ASIC	Detector	Experiment	Reference	Technology	Foundry	Challenge
Microplex	SSVD	Mark II (SLC)	Nucl.Instrum.Meth. A313:63-102,1992	NMOS 5 um	Gould-AMI	N
TEKZ	LPS	ZEUS (HERA)	Nucl.Instrum.Meth. A364:507-515,1995	Bipolar	Tektronix	R, N
DTSC	LPS	ZEUS (HERA)	Nucl.Instrum.Meth. A288:209-211,1990	Rad-hard CMOS	UTMC	R, P
LBIC	Si TKR	SDC (SSC)	IEEE Trans.Nucl.Sci. 42:796-802,1995	Bipolar	Tektronix	R, N, S, P
CDP	Si TKR	SDC (SSC)	IEEE Trans.Nucl.Sci. 44:736-742,1997	Rad hard CMOS	Honeywell	R, P
CAFE	SCT	ATLAS (LHC)	IEEE Trans.Nucl.Sci. 41:1095-1103,1994	Bipolar	AT&T	R, N, S, P
CAFE	SCT	ATLAS (LHC)	IEEE Trans.Nucl.Sci. 49:1106-1111,2002	Bipolar	Maxim	R, N, S, P
ABCD	SCT	ATLAS (LHC)	IEEE Trans.Nucl.Sci. 47:1843-1850,2000	BiCMOS	DMILL	R, N, S, P
ATOM	SVT:	BaBar (PEP 2)	IEEE Trans.Nucl.Sci. 44:289-297,1997	Rad-hard CMOS	Honeywell	R, N
DCAC	CDC	BaBar (PEP 2)	Nucl.Instrum.Meth. A409:310-314,1998	Bipolar semi-custom	Maxim	N, S,
GTFE	TKR	GLAST	IEEE TNS 45, pp. 927-932, 1998	0.5 um CMOS	Agilent	N, P
GTRC	TKR	GLAST	Nucl.Instrum.Meth. A457:126-136,2001	0.5 um CMOS	Agilent	P
LC	SILC	LC		0.25 um CMOS	TSMC	N, P

N = noise, R = radiation hardness, S = speed, P = power

H

Radiation Damage Pedigree of SCIPP Group

SSD Detectors

Change in Effective Donor Concentration
Temperature Effects in Annealing of Radiation Damage
N-on-n detectors
CCE

ASICs

Rad-hard CMOS (UTMC, Honeywell)
Rad-hard Bipolar (Maxim, AT&T, DMILL)
Low-dose effects
SEE effects