Electrical characterization and optimization of silicon carbide p*/n junctions for particle detectors

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Motivations

- Final goal: realization and characterization of a particle detector based on SiC
- Use of a planar technology (no Mesa) ⇒ ion implanted p/n junctions





The research team

- University of Perugia (Italy)
 - Device design and simulation
 - Electrical measurements
- Partner (SiC technology)
 - CNR-IMM Bologna (Italy)
- Collaborations
 - INFN-Italy (SiCPOS project)
 - Cegely Lyon (France)





Outline

- Introduction on SiC properties
- Test diode p⁺/n (and n⁺/p):
 - Technological process
 - I / V and C / V measurements
- Preliminary modeling of SiC detectors
 - Motivations and simulation tool
 - Test diode and calibration
 - Preliminary results
- Conclusions





Silicon Carbide

- large E_g (3-3.3 eV) \longrightarrow very low leakage current
- MIP (Minimum Ionizing Particle) generates 51 e/h pairs per μ m
- radiation hardness (?) (high atomic binding within the material)
- high quality crystals now available
- Schottky barrier detectors have been studied as α-particle detectors (100% of charge collection efficiency (CCE))*

* Nava, Cavallini, Bruzzi, Bertuccio 2000-2002





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SiC Process: p⁺/n



Epi (40 µm) doping: $1 \times 10^{15} \text{ cm}^{-3}$



Al (350 nm) / Ti (80 nm) deposition

Annealing 1000°C in vacuum 2 min



Ion implantation Al⁺ (*a*) 300°C Annealing 1650°C 30 min p^+ doping (0.4 μ m) $= 4 \times 10^{19} \text{ cm}^{-3}$



Optional p⁻ extensions





I-V measurements on p⁺/n diodes



- 75% of diodes have good I-V curves
- V_{BD} is about 4 kV
- Theoretical limit for this device: 5 kV
- A few diodes now available for testing as particle detectors

Diode diameter: [0.3,1] mm

Power diode layout design by INSA-CEGELY, Lyon France



CV measurements













Preliminary I-V measurements on n⁺/p diodes





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Motivations for simulation

- Very high cost of SiC wafers
- Suitability of device simulation for design optimization
- Trade off between SiC wafer quality and available budget

Simulation Tool

- DESSIS ISE-TCAD
 - Discrete time and spatial solution to the fundamental semiconductor equations
 - 6H-SiC model available





Known experimental results: MIP crossing in 4H SiC*

- Bias voltage 500 V
- Induced collected charge: 2000 e⁻
- Noise charge 300 e⁻
- Drawbacks:
 - High number of defects
 - high operating voltage

50 µm 3 mm Ohmic contact Semi-insulating 4H-SiC

Ohmic contact

* M. Rugalla, K. Runge, A. Soldner-Rembold "Particle detectors based on semiinsulating Silicon carbide," Nuclear Physics B, vol. 78 (1999) 516-520



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Heavy Ion crossing modeling available in DESSIS ISE-TCAD



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Model Calibration

Ohmic contact $p^+=10^{19} \text{ cm}^{-3}$ $n = 10^{12} \text{ cm}^{-3}$

Ohmic contact

• Signal: 3 completely depleted diodes:



- <u>Noise</u>: agreement between measured and simulated leakage current densities
- Calibration with experimental CCE from a MIP still to be done (data are not yet published)





Model parameters

Electron mobility (cm ² /Vs)	380
Hole mobility (cm²/Vs)	70
Relative dielectric constant	9.66
Intrinsic concentration <i>n_i</i> @300K (cm ⁻³)	1.6×10 ⁻⁶
Saturation velocity (cm/s)	2×10 ⁷
Electron lifetime (ns)	100
Hole lifetime (ns)	20





Test diode

- p+/n diode
- 4 technological parameters:
 - p+ depth between 0.45 and $\textbf{3}~\mu\text{m}$
 - p+ doping between 10^{18} and 10^{20} cm⁻³
 - epi doping between 10¹⁴ and 10¹⁵ cm⁻³
 - n epi thickness between 10 and $\textbf{40}~\mu\text{m}$





p⁺/n diode output signal



epi doping (40 μ m) = 10¹⁵ cm⁻³ p⁺ doping (0.45 μ m) = 4×10¹⁹ cm⁻³





Collected Charge vs. junction depth

- Epitaxial layer:
 - thickness = 40 μ m
 - doping = 10¹⁵ cm⁻³
- p^+ doping = 4×10^{19} cm^{-3}
- CC increase due to:
 - 51 e/h pairs per μ m
 - minority carrier diffusion length \geq than junction depth



junction depth [µm]

Note: the charge generated in the epi layer is about 2000 e/h
 ⇒ charge collection from the substrate! Calibration problem still
 to be solved (also present in next slides)





Collected Charge vs. p⁺ doping

- Epitaxial layer:
 - Thickness = 40 μ m
 - $\text{ doping} = 10^{15} \text{ cm}^{-3}$
- junction depth:
 - 2 μm and 3 μm
- Reasons for increase at small junction depth not well understood so far





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Collected Charge vs. epi n doping

- epi thickness = $40 \,\mu m$
- junction depth = $2 \mu m$ p^{+} doping = 4×10^{19} cm^{-3}
- CC decrease to:
 - decrease of depleted region for constant V_{R}
 - transient behavior of the CC due to displacement current $\varepsilon_0 \cdot dE/dt$





Collected Charge vs. epi n depth



- Epi doping = 7×10^{14} cm⁻³ (depletion depth 12 μ m)
- Junction depth = 2 μ m p⁺ doping = 4×10¹⁹ cm⁻³
- CC increase might be due to:
 - smaller recombination likelihood
 - transient behavior of the CC due to displacement current $\varepsilon_0 \cdot dE/dt$





Conclusions

- p⁺/n junctions have been realized and electrically characterized. Good forward and reverse characteristics have been obtained
- SiC detectors have been analyzed and simulated:
 - charge collection from the substrate. Calibration problem still to be solved;
 - technological parameters have been studied. The epi doping and the epi depth are the most important parameters. junction depth is also an important parameter;
 - an average price wafer seems to be suitable for the realization of a SiC detector.





Future developments

- Analysis of the lateral crossing of a MIP
- DLTS and CCE analysis will be carried out on the realized diodes and results will be compared with the simulations
- Radiation hardness will be verified
- New SiC detectors will be realized taking into account the simulation results





Appendix





Experiments at CERN



- Large Hadron Collider (LHC) experiment (upgrade)
- Fast hadron fluences above 10^{16} cm⁻² (after 10 years)
- Current silicon technology is unable to cope with such an environment
 - Unreachable full depletion voltage
 - Very high leakage current
 - Poor charge collection efficiency





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Silicon Detectors

 Minimum Ionizing Particle (MIP) generates in Si 80÷90 e/h pairs per micron

