

CiS - Technologies for Radiation Hard Silicon Detectors

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April 2003: Restart of the clean room and wafer processing facilities
after move to new buildings in Erfurt

- Equipment
- Processing capabilities
- Design pad-diode
- Radiation Hard Detectors:
 - DOFZ, epi
 - Defect engineering



Equipment & processing capabilities

- 4 inch n- or p- typ silicon wafer, single or double-sided polished
 - double side process and test equipment
 - Automatic coating and developing cluster for double-side processing
 - Projection mask aligner, projection photolithography
 - Spray coating equipment
- ...
- partly 6 inch compatible
- up to 2000 detector wafer p.a.
- high ohmic (1 - 30 kOhmcm) STFZ or DOFZ
- CZ (>600 Ohmcm), epi (for example 50 Ohmcm) on CZ
- **Thickness:** (200 µm) ... 250 µm ... 285 µm ... 300 µm ... 500 µm ... (800 µm)





High temperature facility

Oxydation
Oxygen enrichment

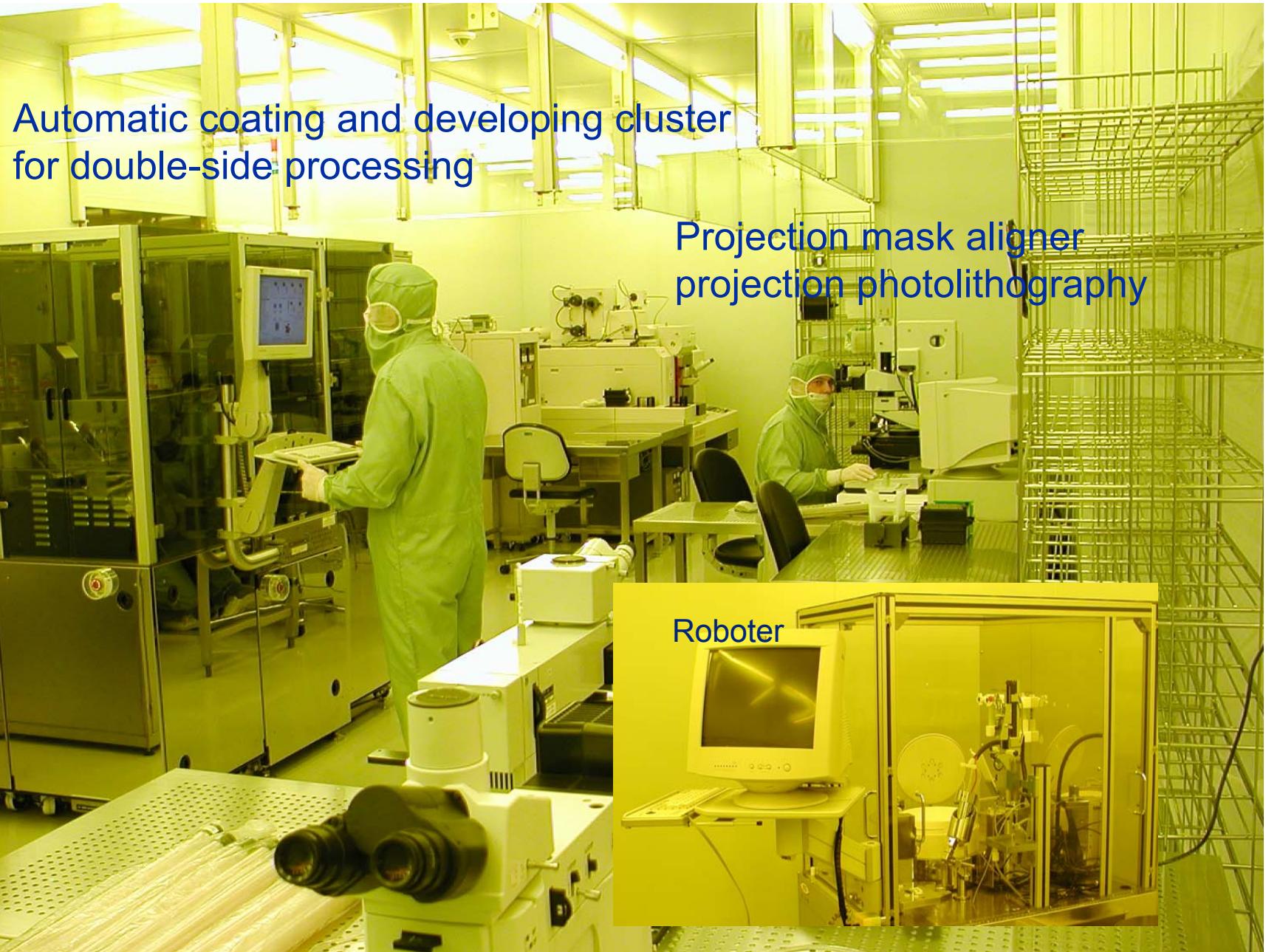




LP - CVD

SiO_2 , SION, Si_3N_4
stress reduced
Poly-silicon







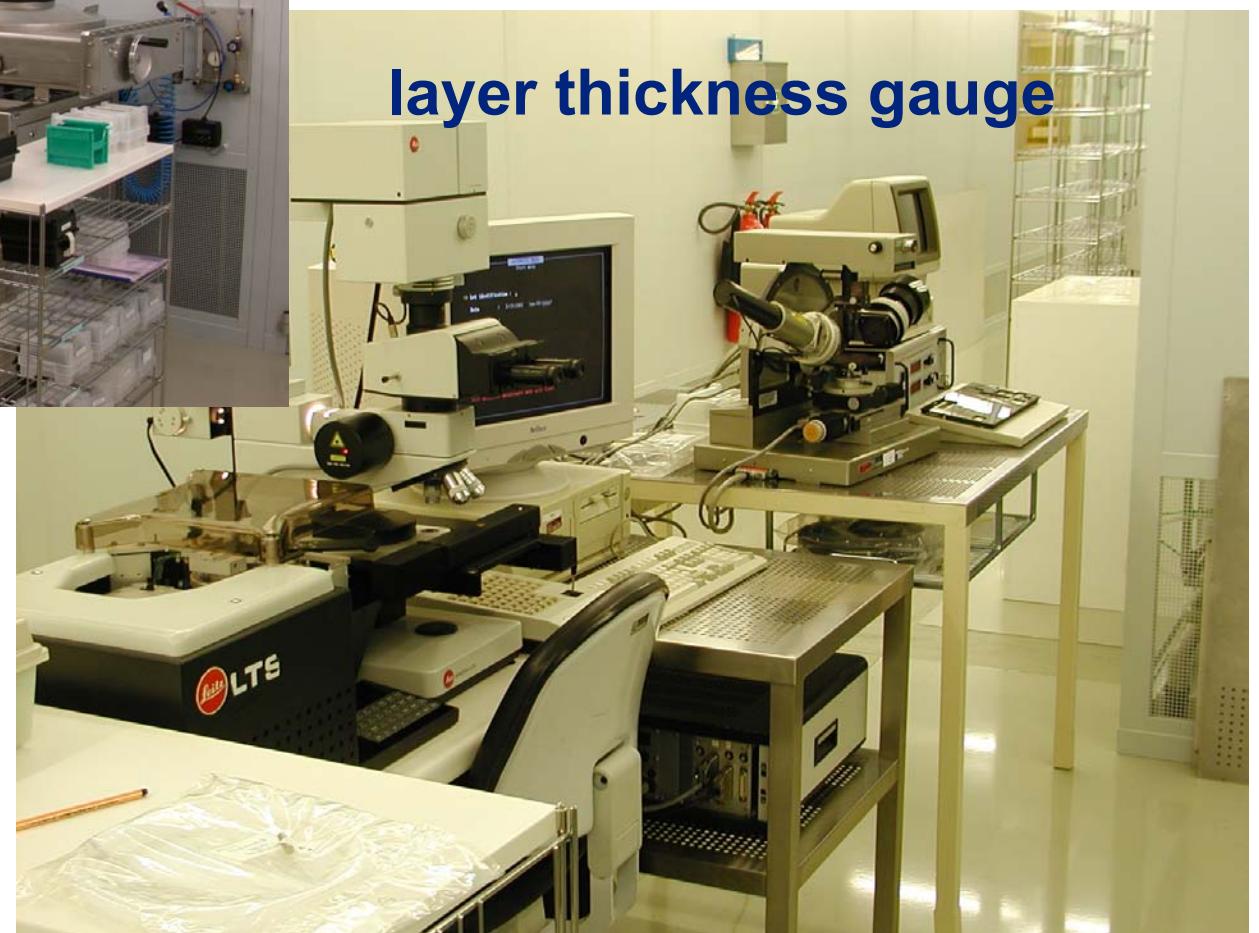
Improved quality of

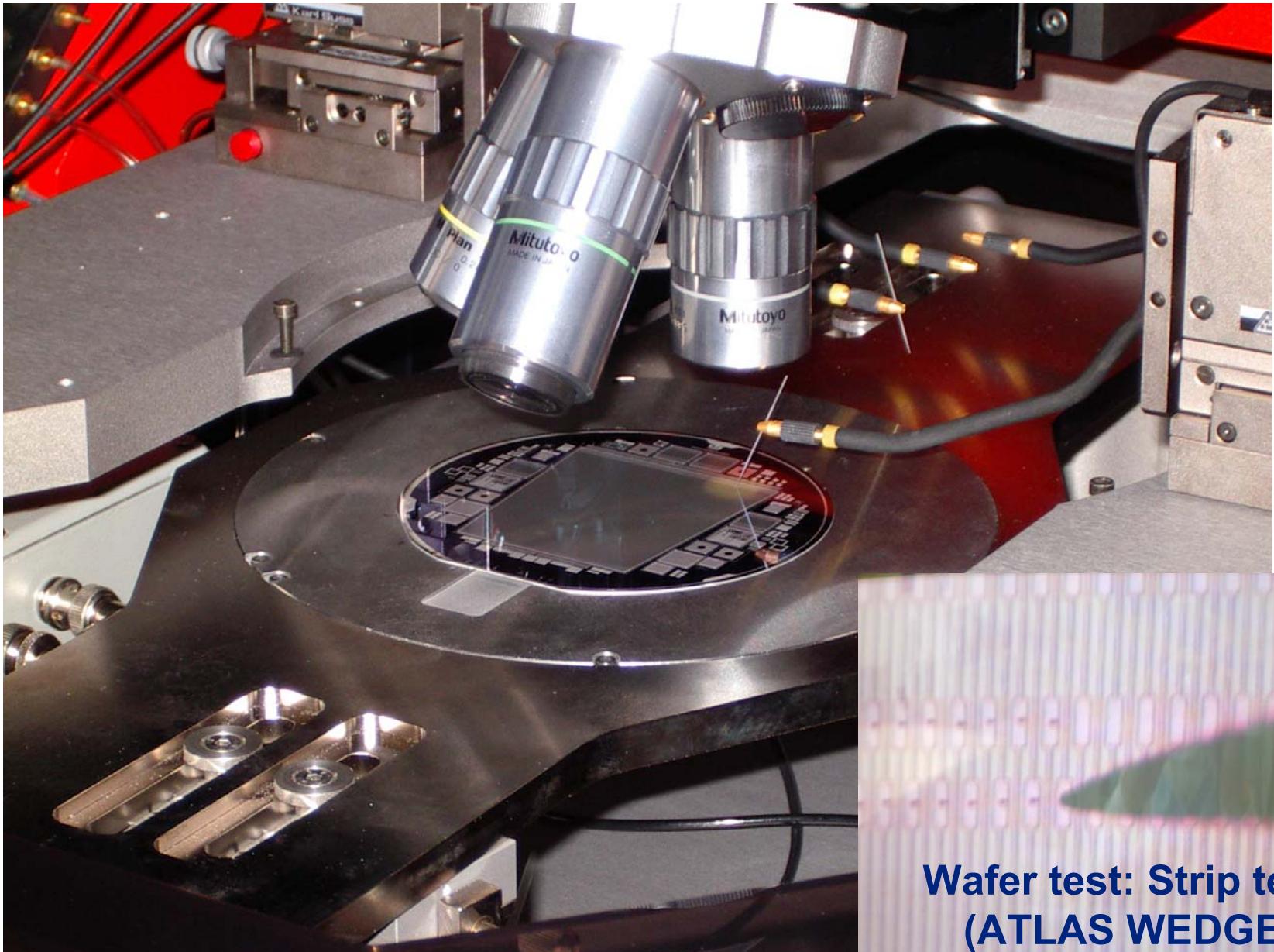
- gases
- photoresist (less Na ions)
- DI water

Improved conditions for

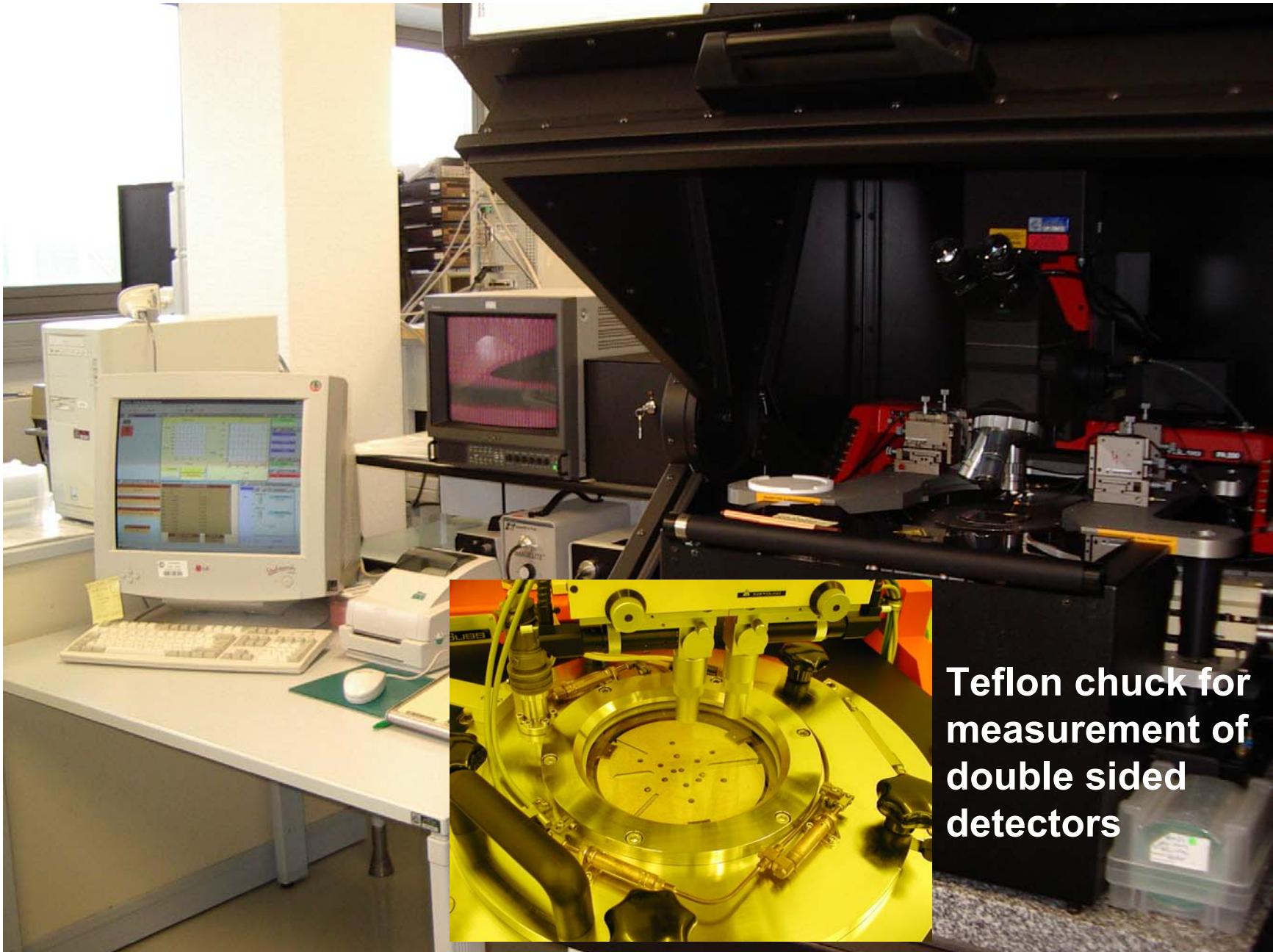
- wafer cleaning
- wet etching
- photoresist wet structuring







**Wafer test: Strip test
(ATLAS WEDGE)**

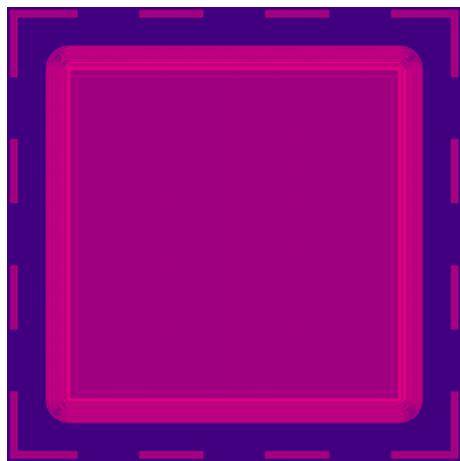


**Teflon chuck for
measurement of
double sided
detectors**

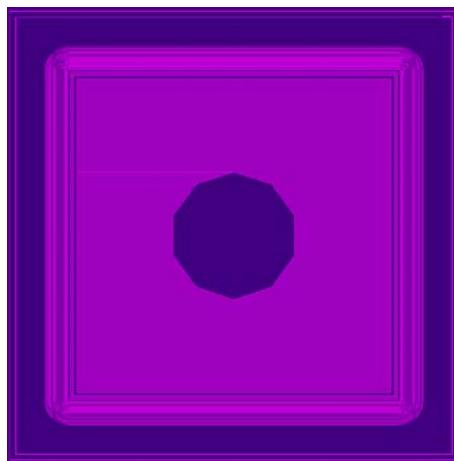
2nd RD50 - Workshop on Radiation hard semiconductor devices
for very high luminosity colliders

18. - 20. May 2003

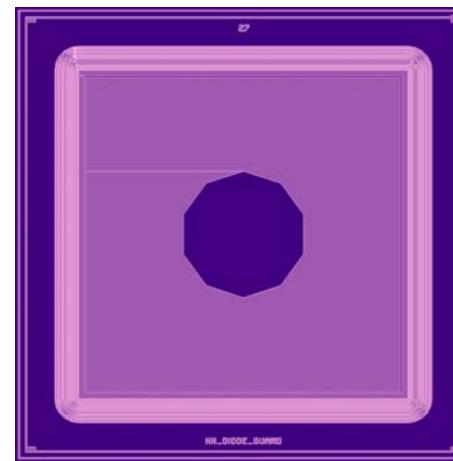
pad - diode



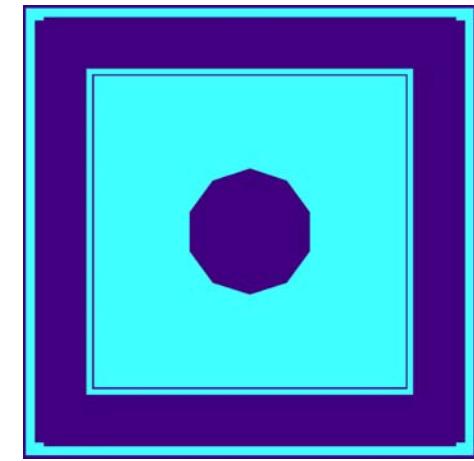
Mask A:
boron implantation



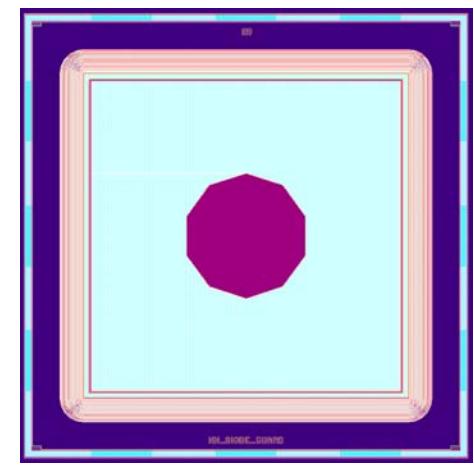
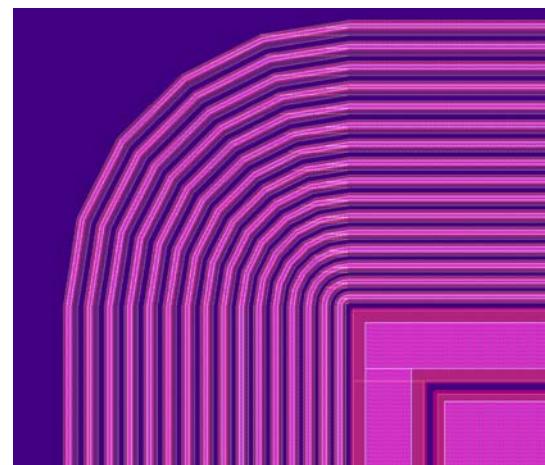
Mask C:
contacts
opening of field oxyd



Mask D:
metal AlSi 1 μ m



Mask E:
passivation opening



pad - diode details

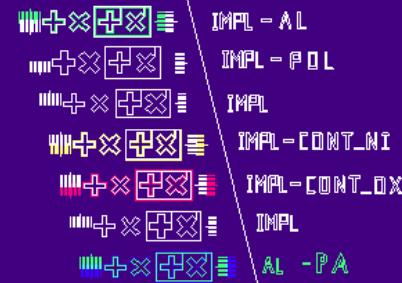
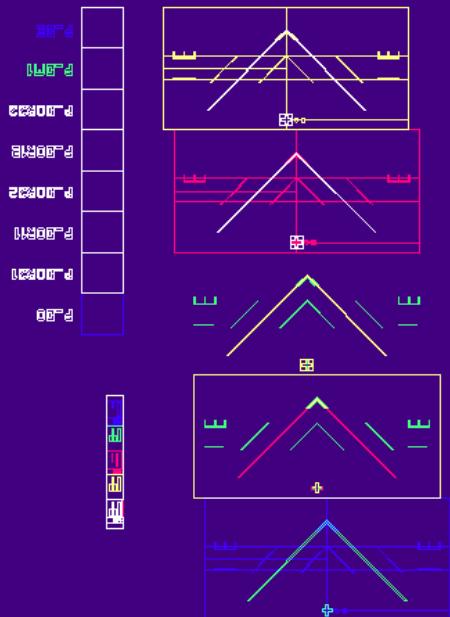
Multi-guard ring structure:
16 scaled rings

Mask A

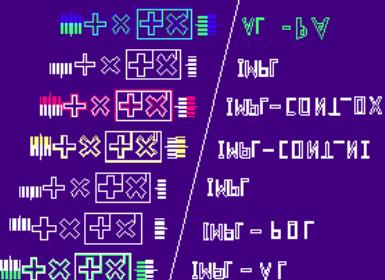




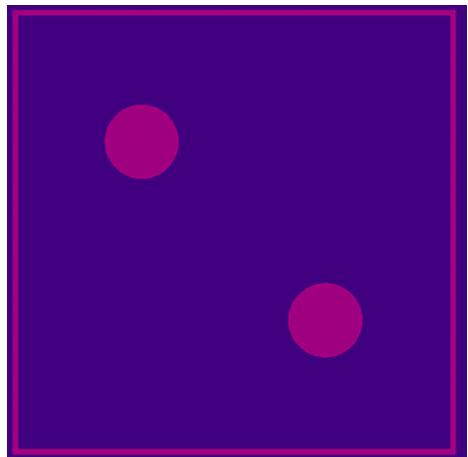
Structures for automatic alignment



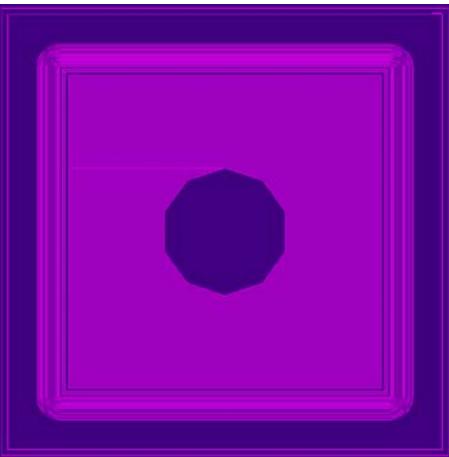
Optical control
structures
of mask alignment



Test structures details



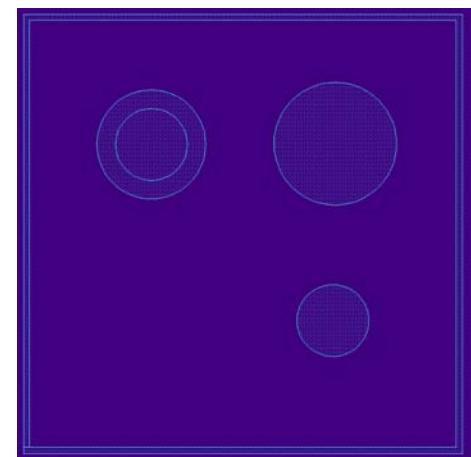
Mask A:
boron implantation



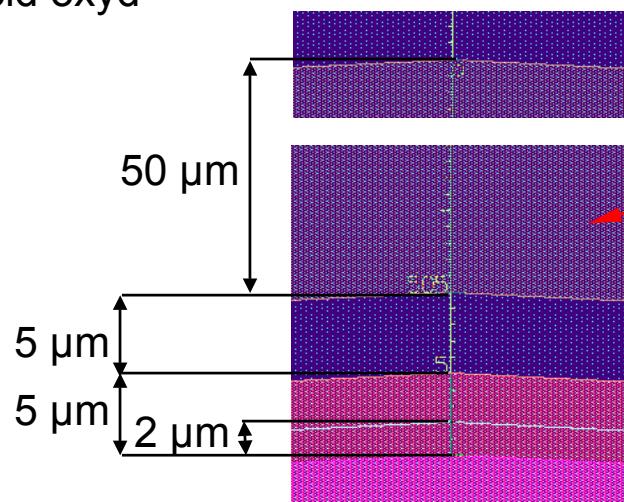
Mask C:
contacts
opening of field oxyd



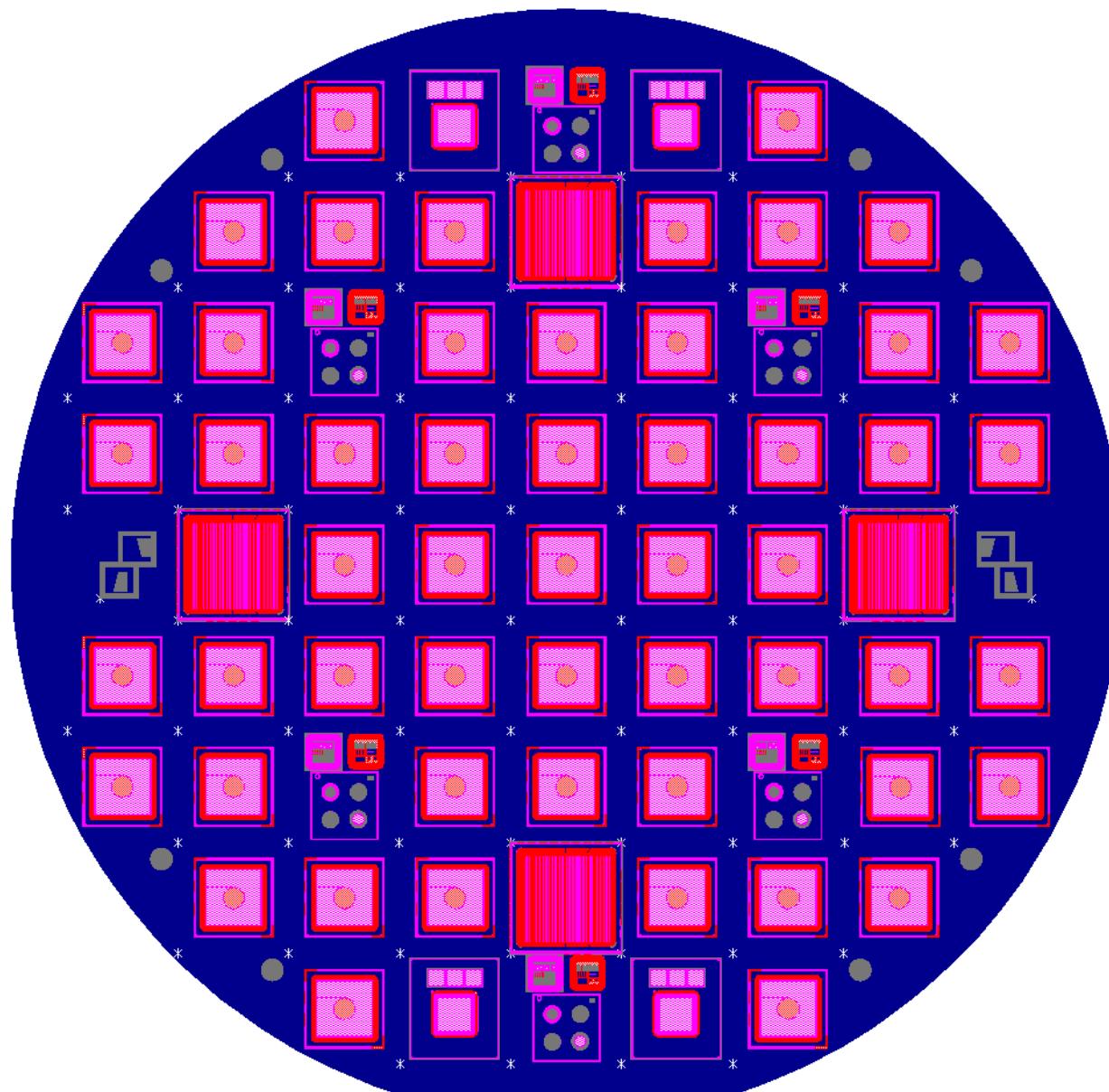
Mask D:
metal AISi 1 μm



Mask E:
passivation opening



Test wafer SDTW01-2



Layout: SRD wafer

1	2
8	7
6	5
4	3
9	10
24	23
22	21
20	19
18	17
16	
25	26
27	28
29	
38	37
36	35
34	33
32	31
30	
39	40
41	42
43	44
45	
51	50
49	48
47	46
52	53

= border chips, not usable

= pad-diode chips

= pad-diode chips, first measurements

flat

SRD - test wafer program

2000 - 2002

	n/P, FZ <100>, 1-6 kOhmcm (Wacker)	n/P, FZ <111>, 1-6 kOhmcm (Wacker)	n/P, FZ <111>, 4-7 kOhmcm (Topsil)
Standard	26 wafer	28 wafer	6 wafer
DOFZ 24h	22 wafer	22 wafer	
DOFZ 48h	18 wafer	18 wafer	
DOFZ 72h	24 wafer	24 wafer	12 wafer

Used technology:
like
ATLAS WEDGE
W12

	highohmic CZ >600 Ohmcm (Sumitomo)	CZ+epi
Standard	48 wafer	9 wafer

Next steps:

- MCZ
- CZ+epi
- FZ <111>, 3-4 kOhmcm

Results of processing of SRD and oxygen enriched ATLAS detectors (> 250 wafer) (ca 900 wafer)

- We have recognized:
 - quality and yield of the DOFZ detectors fundamentally depends of
 - charge of the wafer delivery (manufacturer/distributor, ingot [region])
 - for example: since 2002 Wacker wafer have saled by Wafernnet -> significant deterioration (for STFZ wafer it was far less important)
 - grinding and polishing of the wafers has also a basic influence
 - surface defects, metal contaminations by grinding and polishing pastes
 - the effects of different behavior of various wafer zones
 - (ca 3“ center, outer zone)
this effect we have seen particularly at DOFZ wafers
 - high ohmic CZ wafers from Sumitomo: two strongly different qualities
 - Thesis: denuded zones play a important rule
in respect of wafer processing
=> defect engineering in various layers
could be conceivable, advisable



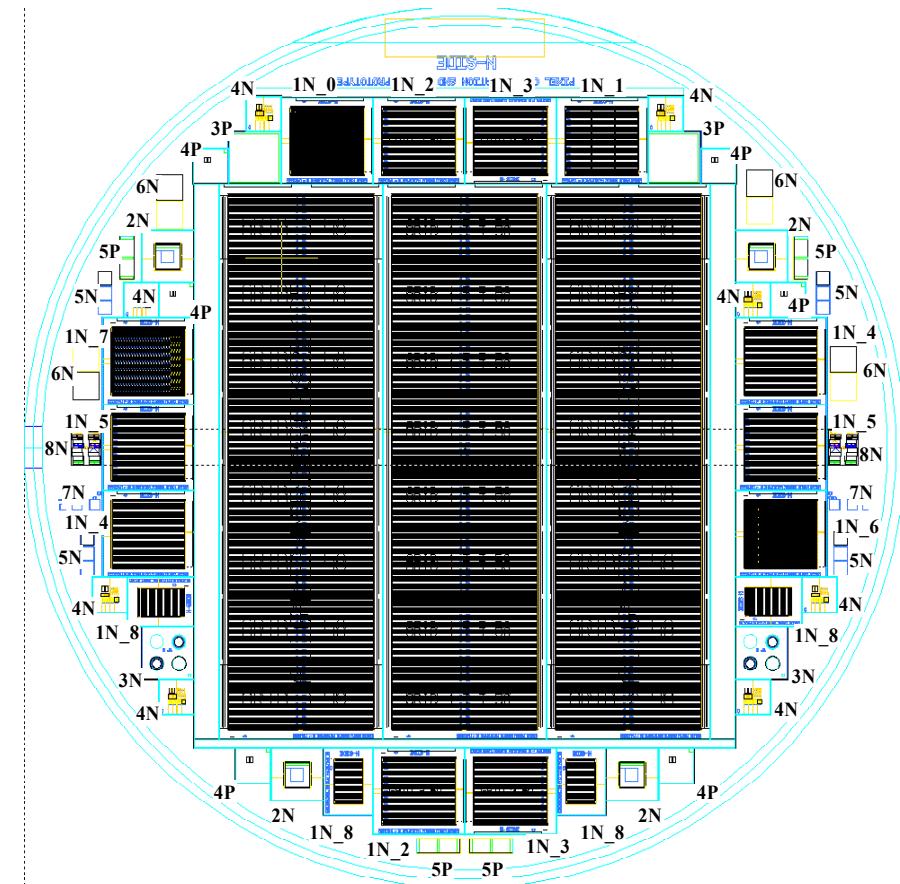
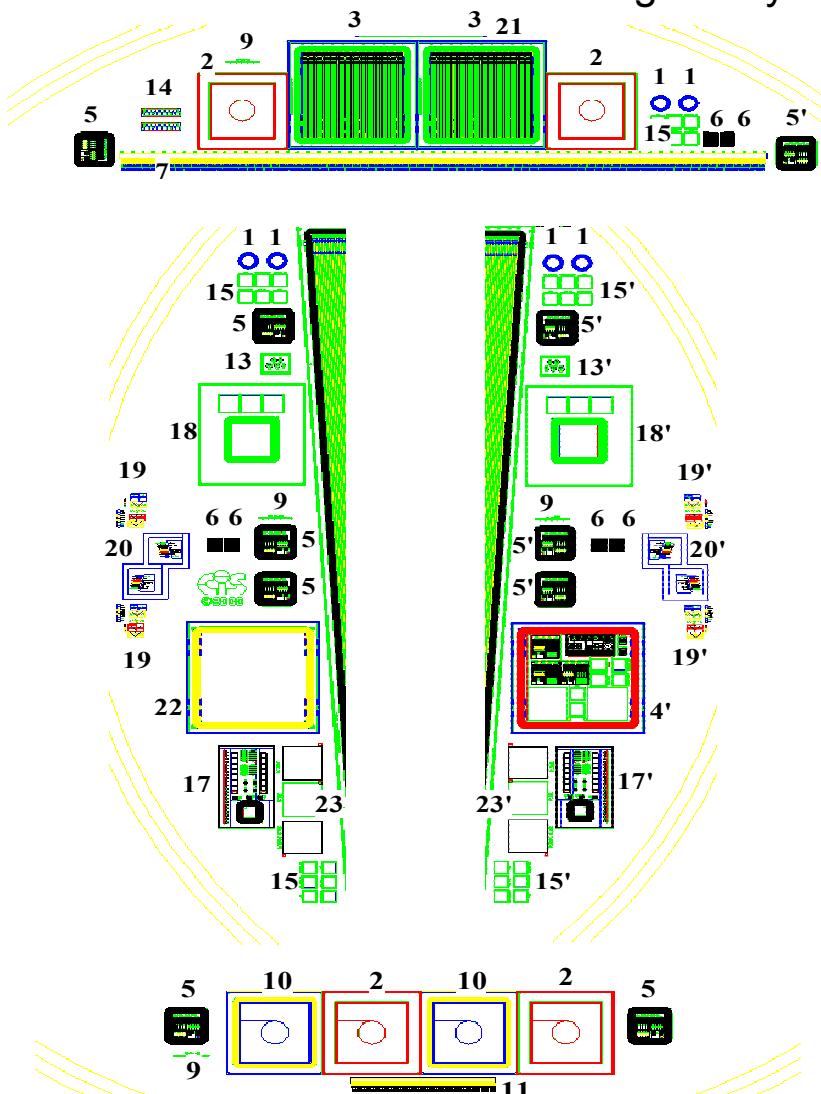
What CiS can offer for Rd50?

- Processing of wafers for R&D
 - HCZ/MCZ, STFZ, DOFZ.
 - oxygen enhancement by high temperature diffusion (1150C, N₂, 16 - 72 hours; if necessary also longer temper times for R&D)
 - double side processing, structuring of back side metalization (mesh)
- some additional services:
 - sawing, bonding (US, thermo compression, stud bumping), mounting & housing
 - mask design, mask set (fabrication by ML&C Erfurt)
 - test structure design
- "bad" wafers of detector production, for instance ATLAS PIXEL and ATLAS WEDGE (if the ATLAS collaboration / CERN agrees):
 - 24 hour DOFZ - pad-diodes, mini strip-detectors, test structures (gated-diodes,...) perhaps "one tile" - pixel wafer (n/P, <111>, 2 - 5 kOhmcm)



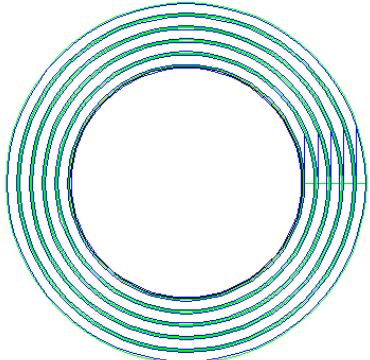
ATLAS Test structures

designed by MPI Halbleiterlabor Munich



gate controled diode:

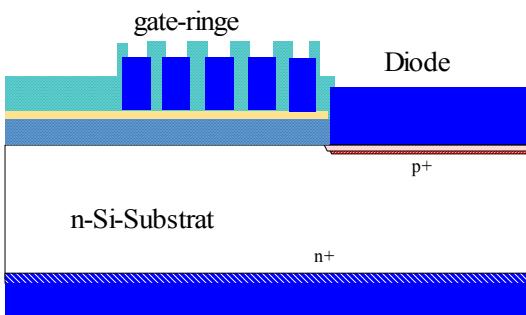
kreisförmige Diode ($\varnothing=1\text{mm}$),
ganzflächig geöffnet und mit Metall bedeckt
umgeben von 5 Metallringen auf Feldoxid und Nitrid



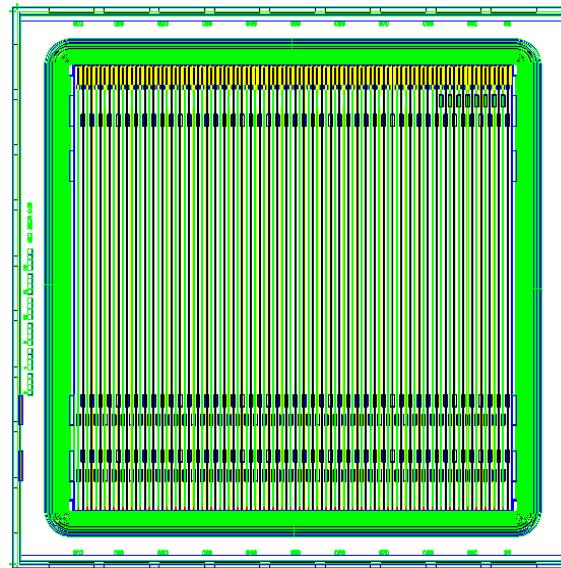
Gruppe: TEST_DO

ws: p+ - Diodengebiet $\varnothing=1\text{mm}$
ganzflächig kontaktiert: Kontaktloch rt: $\varnothing=1\text{mm}$
Metall: gn: $\varnothing=1,01\text{mm}$ über der Diode und $5\mu\text{m}$ über A-Kante
mit bias- p- Implantation: $\varnothing=1,004\text{mm}$
Passivierungsöffnung: $\varnothing=0.99\text{mm}$ ($5\mu\text{m}$ von A-Kante entfernt)

5 Metallringe auf 300nm Feldoxid und 50nm Nitrid
Breite der Ringe je $50\mu\text{m}$, Abstand $5\mu\text{m}$
Passivierungsöffnung mittig und $40\mu\text{m}$ breit



BABY_DET_CIS

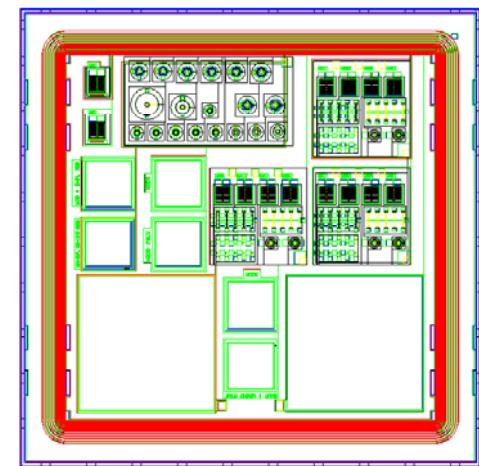


98 parallele Streifen mit integriertem bias-Widerstand (ge,am oberen Ende der Streifen) und Auslesekondensator analog W21-Detektor

- Länge der p+ -Gebiete 7.99mm , Breite $18\mu\text{m}$,
- umlaufend um p+ -Streifen mit $0.1\mu\text{m}$ Abstand p-Bias-Implantation mit $2.7\mu\text{m}$ Breite
- Abstand der Streifen (p+ -Gebiete): $62\mu\text{m}$
- Kontakt zu p+ je am oberen und unteren Ende der Streifen (Metall: $65 \times 75\mu\text{m}^2$ oben, $18 \times 40\mu\text{m}^2$ unten)
- Auslesekondensator Metall über p+ auf Implantationsoxid und Nitrid Länge $7,508\text{mm}$, Breite $19\mu\text{m}$ (mit je 3 Pads, unten 2 und oben 1, Metall $69 \times 213\mu\text{m}^2$):
-

Guard-Ring_Struktur wie W21-Detektor, die bias-Widerstände laufen gegen den bias-Ring, der, oben links und rechts neben den Pads der Auslesekondensatoren kontaktiert werden kann.

TEST_MULTI_PURPOSE

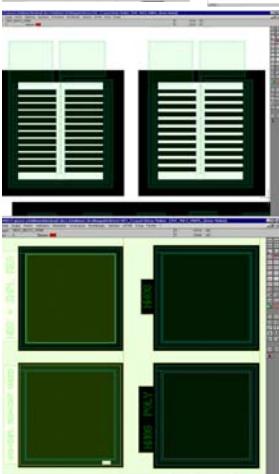


Oben-Mitte: kreisförmige Dioden mit umlaufender Guardringdiode in unterschiedlichen Abständen (Detailbild-A) und MOS-Tristoren (B)
Oben-rechts und Mitte/Mitte-rechts:
 4-Draht-Messung p+ -Streifen 4,10,20,30 und 40 μ m Breite, 2-Draht-Messung bias-Streifen 5.2, 11.2, 21.2, 31.2 und 41.2 μ m, kreis-förmige Dioden mit umlaufender Guardringdiode und bias-Brücke (C), oben: Kammförmig Diode mit Metallabdeckung für die Untersuchung der Beeinflussung der Randeigenschaften der Diode durch eine Oberflächenladung auf dem Oxid (D)
Oben-links: Kammdiode ähnlich Oben-rechts
Mitte-links: MOS-Strukturen (E)
unten-links: Metall über p+ und bias-Impl auf Impl-Oxid ohne Nitrid
unten-rechts: Metall über p+ auf Impl-Oxid mit Nitrid
unten-mitte: Metall und Metallring über Substrat auf Feldoxid+Nitrid (oben) und mit Metallring mit kl. p+-Gebiet zum absaugen der generierten Löcher (unten)



von links nach rechts:
 Detailbild A, B, C

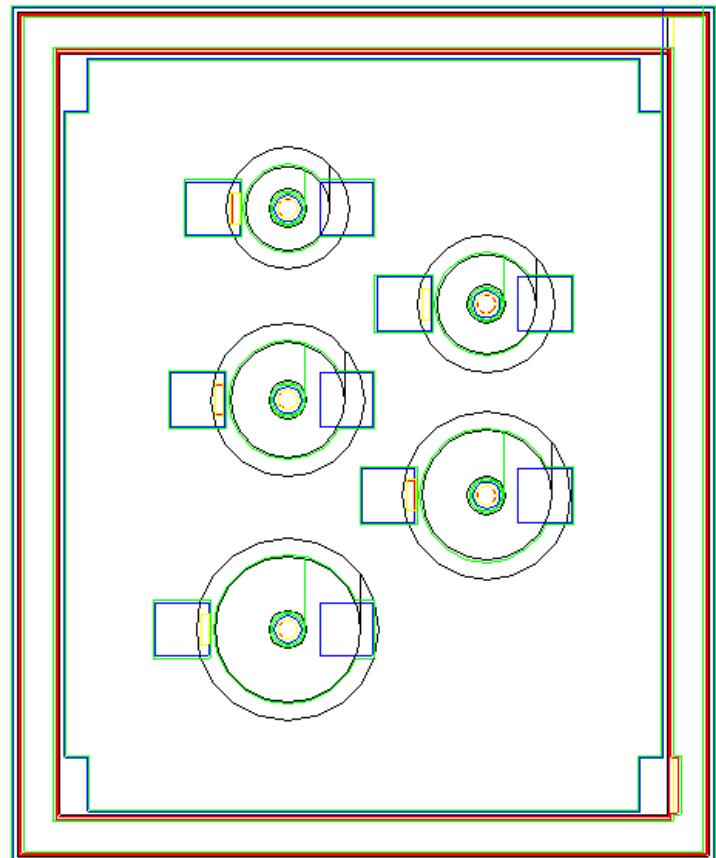
Detailbild D



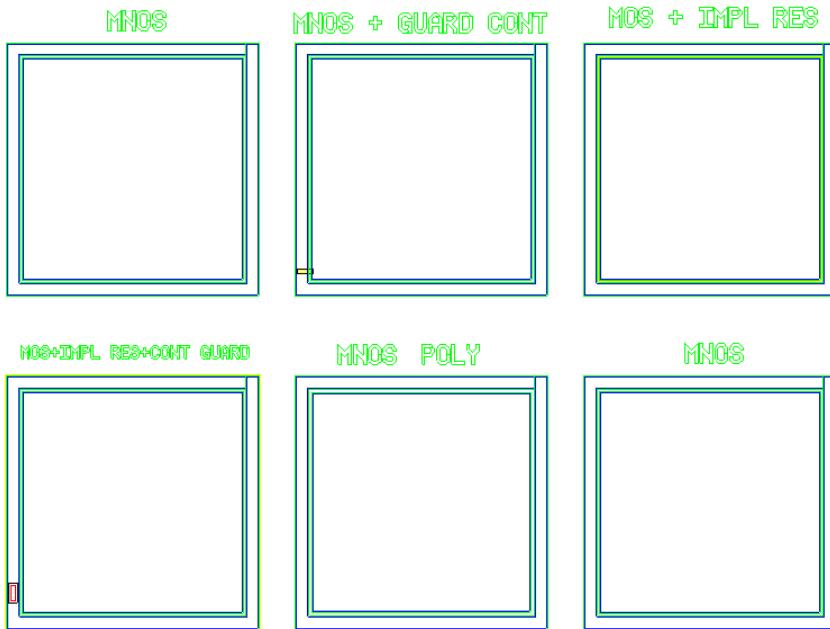
Detailbild E:
oben links: Metall über bias-Implantation auf Feldoxid über Substrat auf Feldoxid+Nitrid
oben rechts: Metall über Substrat auf Feldoxid+Nitrid mit Metallring über Substrat auf Feldoxid+Nitrid
unten links: Metall und Metallring über bias-Implantation auf Feldoxid Metallring mit kl. p+-Gebiet
unten rechts: Metall über Substrat auf Feldoxid+Nitrid mit Metallring über Substrat auf Feldoxid+Nitrid (C???)

ts_most_p_csem

5 MOS-Transistoren mit unterschiedlichen Gatelängen



MOS_block



oben links/ unten rechts: Metall $1 \times 1 \text{mm}^2$ und Metallring (Breite $60\mu\text{m}$, Abstand $10\mu\text{m}$) über Substrat auf Feldoxid + Nitrid

oben Mitte: Metall $1 \times 1 \text{mm}^2$ und Metallring (Breite $60\mu\text{m}$, Abstand $10\mu\text{m}$) über Substrat auf Feldoxid + Nitrid

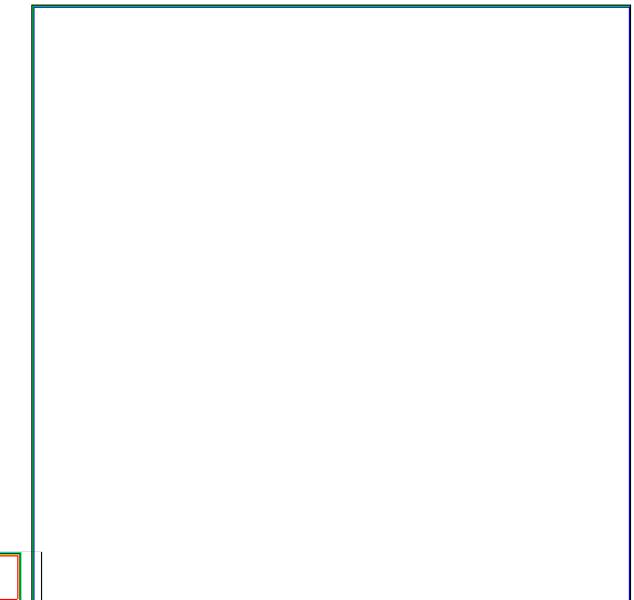
Metallring , Metallring ist mit kl. p+ -Gebiet bebunden, um in tiefer Verarnung Minoritäten abzusaugen

oben rechts: Metall $1 \times 1 \text{mm}$ über bias-Implantation (nicht kontaktiert !) auf Feldoxid und Metallring auf Feldoxid+Nitrid: (Serienschaltung MOS und bias-Impl.-Diode)

unten links: Metall $1 \times 1 \text{mm}$ und Metallring über bias-Implantation auf Feldoxid Metallring. Metallring ist mit p-bias -Implantation verbunden

unten Mitte: Metall $1 \times 1 \text{mm}$ über Substrat auf Restfeldoxid (C im Feldoxid) und Metallring auf Feldoxid+Nitrid

ts_nioxbreak_p



MOS-Struktur: Metall ($2.99 \times 2.99 \text{mm}^2$) über p+ - Gebiet auf Implantationsoxid + Nitrid

Metall ist ganzflächig geöffnet
Das p+ - Gebiet ist unten-links kontaktierbar

RD50 additional remarks

- Common mask set vs. CiS projection lithography
- Technology key parameters may be coordinated:
 - implant dose
 - annealing parameters
 - process variations of lateral structures
(distortion, undercutting, ...)



Our next R&D projects

- Super Radiation Hard Silicon Detectors (Surad)
 - wafer concept: DOFZ, CZ + epitaxial layers (perhaps variation of the epi-layer thickness resp. resistivity)
 - defect engineering
 - oxygen, carbon, hydrogen, ...
 - zone engineering (denuded zone engineering, bulk layers with various defect concentration [especially oxygen])
 - studies of precipitations: perhaps making of free zone of [O]-precipitations
 - optimization of process parameters + processing steps vs. behavior
 - problem: epi-layer double-side devices
 - Monitoring wafer: various test resp monitoring structures:
 - radial distribution of the behavior of some electrical parameters
- Analysis by Hamburg University, MPI Halle, ?
- Microskopic analysis (microstructure also in bulk: HREM, ...) of wafers before and after various processing steps