Tracker Upgrades for Super-LHC

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19/10/08

- Introduction
- Current ATLAS and CMS Trackers
- Upgrade Layout and Occupancy
- Upgrade Radiation Issues
- Mechanics, Services and Material
- Conclusions

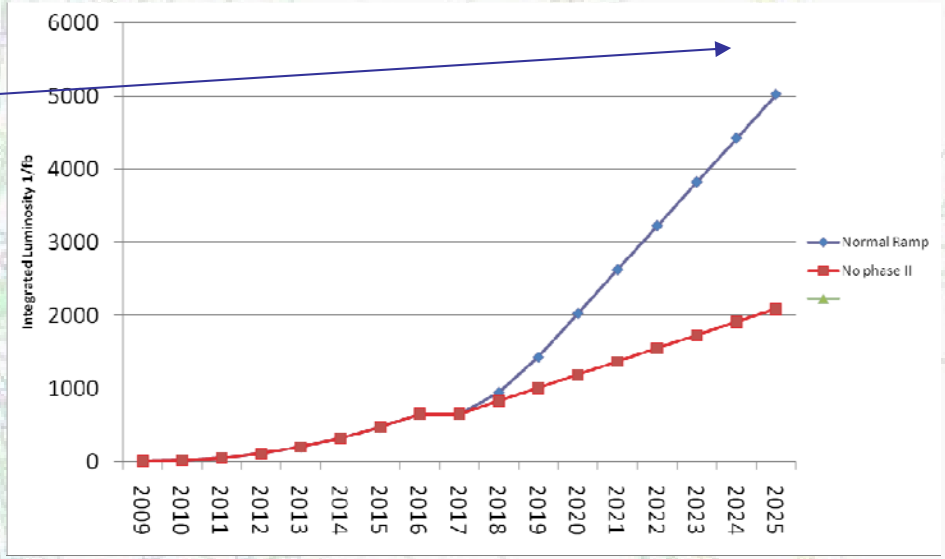
Thanks due to Jordan Nash, Geoff Hall and Mark Raymond of CMS, Chris Parkes and Themis Bowcock of LHCb and numerous colleagues in ATLAS and RD50

Introduction

To keep ATLAS or CMS running beyond ~10 years the trackers will have to go.
(Current trackers designed to survive up to 700 fb^{-1} ≈ 10Mrad in strip detectors)

For the luminosity-upgrade the new trackers will have to cope with:

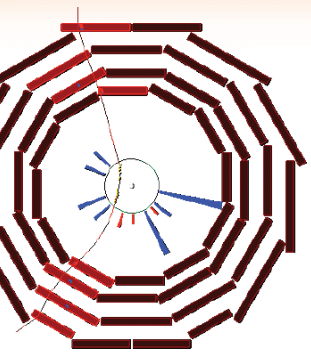
- **much higher integrated doses (need to plan for 6000fb^{-1})**
- **much higher occupancy levels (up to 400 collisions per BCO)**
- **Installation inside an existing 4π experiment**

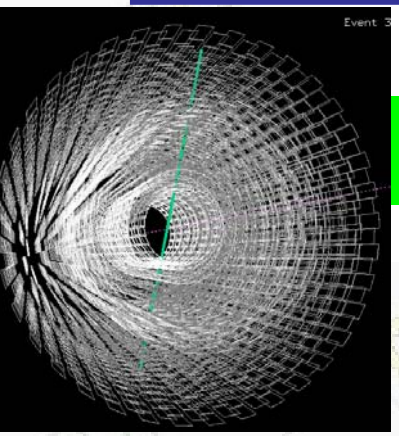


- **Budgets are likely to be such that replacement trackers, while needing higher performance to cope with the extreme environment, cannot cost more than the ones they replace**

To install a new tracker in 2017, major R&D effort already required.
(Note the ATLAS Tracker TDR April 1997; CMS Tracker TDR April 1998)

CMS: The Compact Muon Solenoid





HCAL

Muon chambers

Tracker

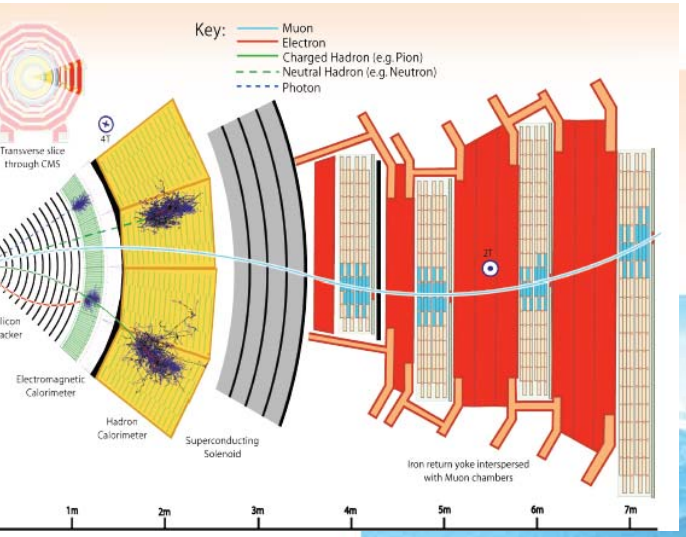
ECAL

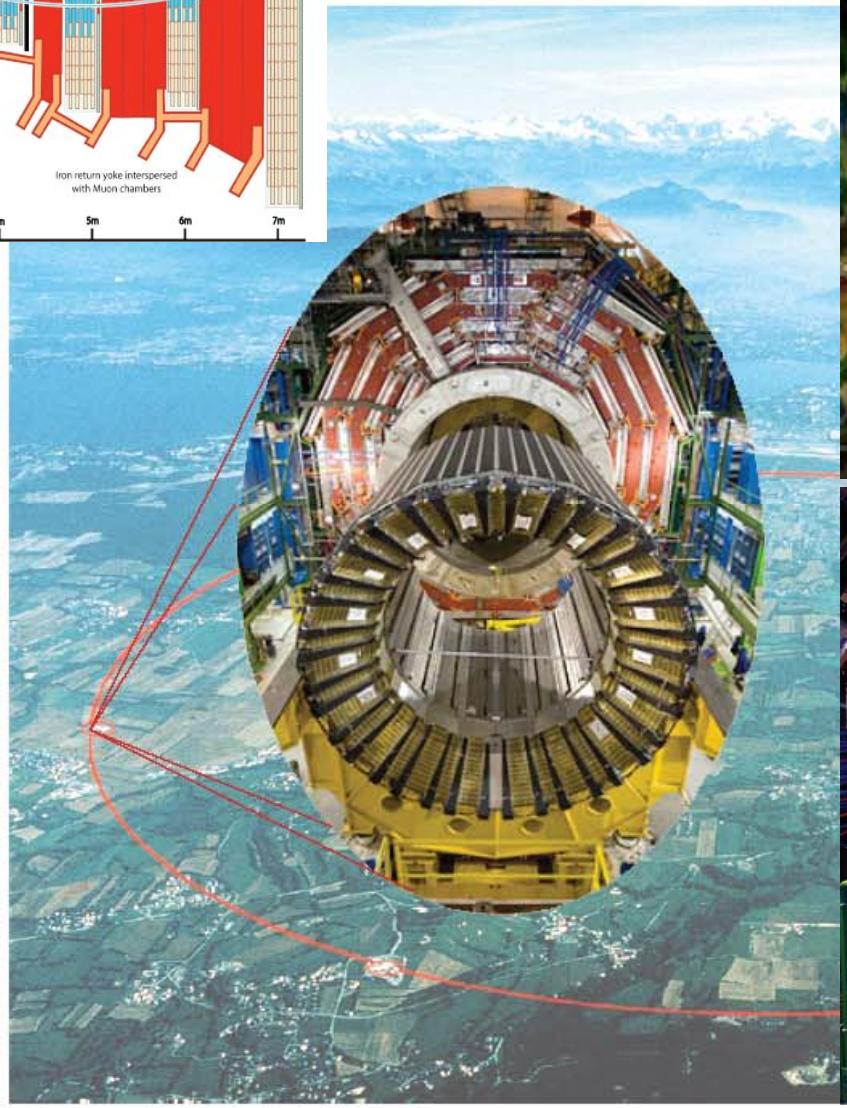
4T solenoid

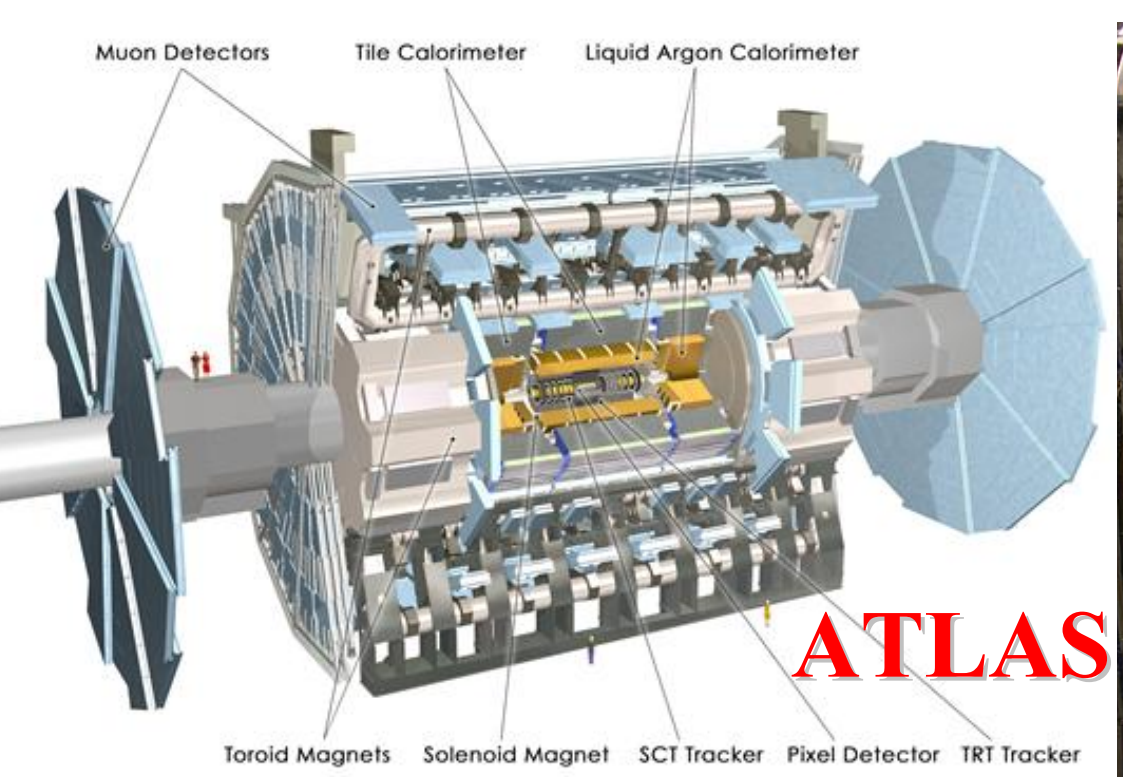
Total weight: 12,500 t
Overall diameter: 15 m
Overall length 21.6 m
Magnetic field 4 T

15,148 modules making ~210m^2 of silicon microstrips

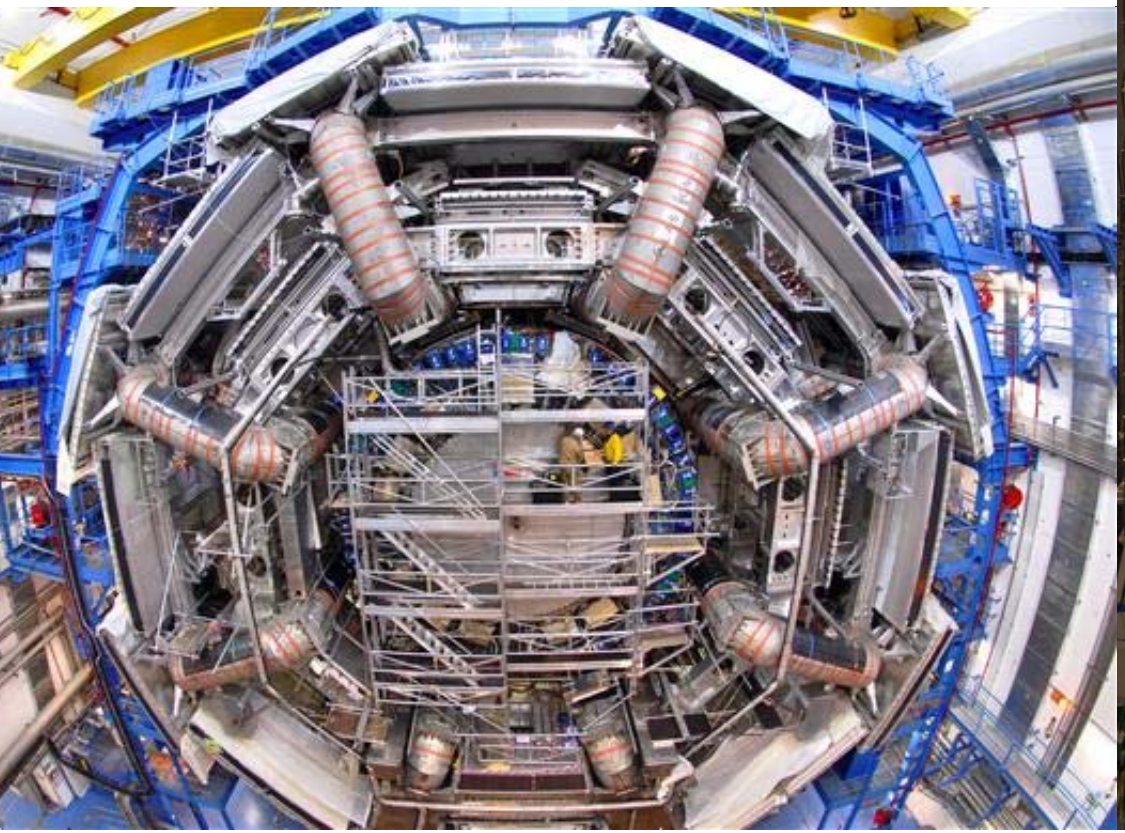
CMS Tracker Installation

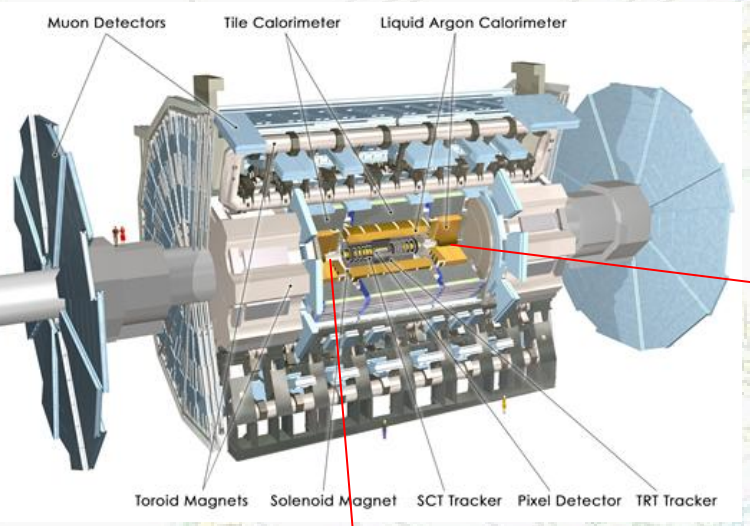






ATLAS Installation

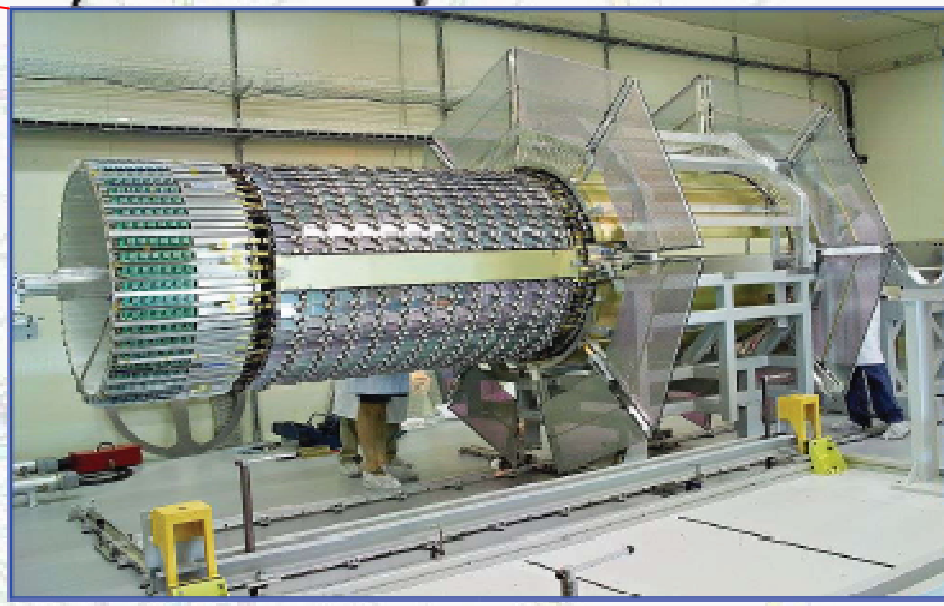




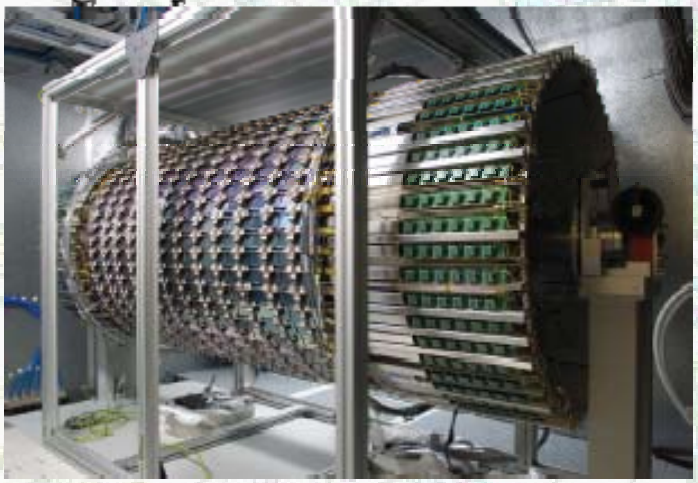
ATLAS SCT

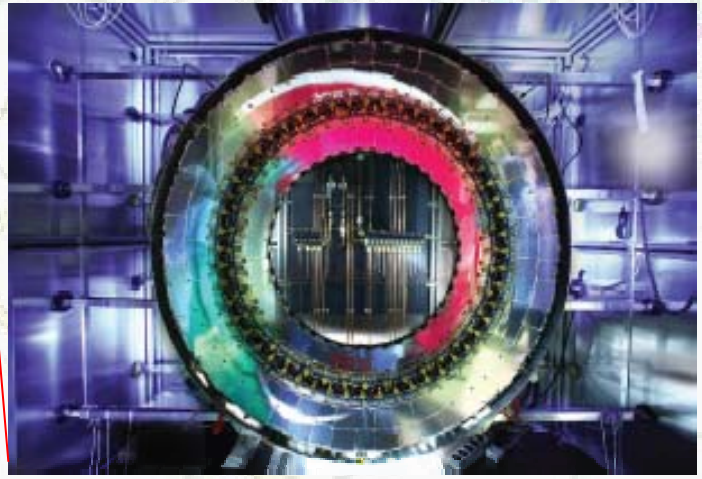
(61m^2 of silicon microstrips)

Sept. 2005: outer layer in thermal enclosure



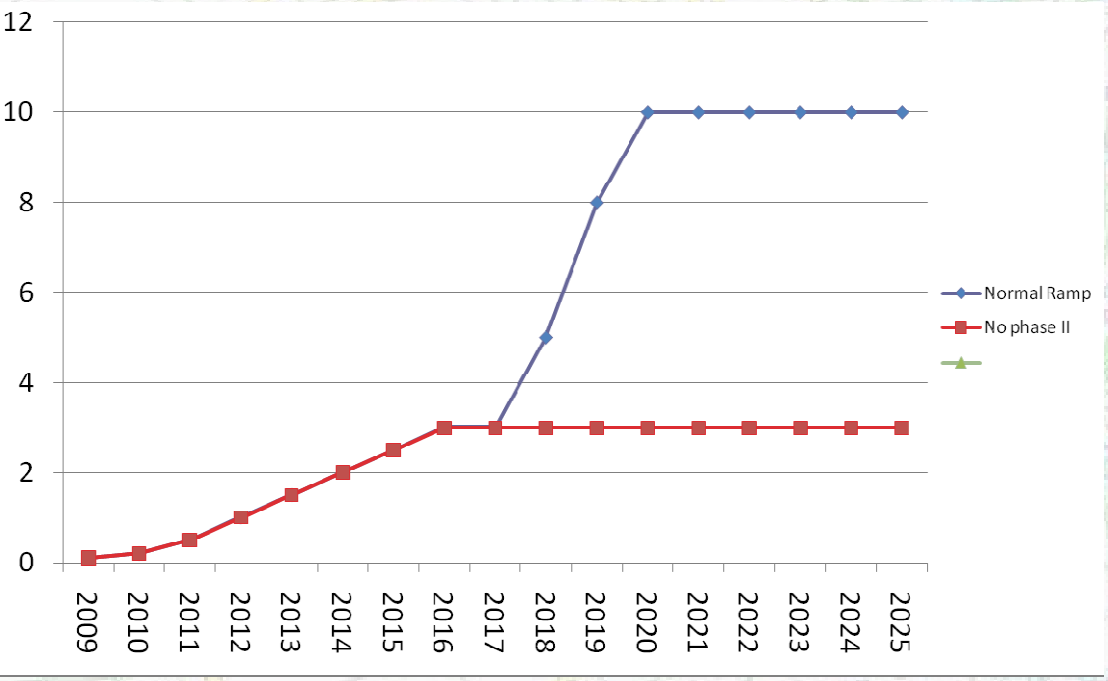
Single cylinder tests





Dec. 2006: inner layer insertion

LHC Luminosity Upgrade Plans



Note that the table assumes L=60 fb^{-1} at 1×10^{34} $cm^{-2}s^{-1}$ but if machine works well we could get L=100 fb^{-1}/year at 1×10^{34} $cm^{-2}s^{-1}$ in 2012

Normal Ramp

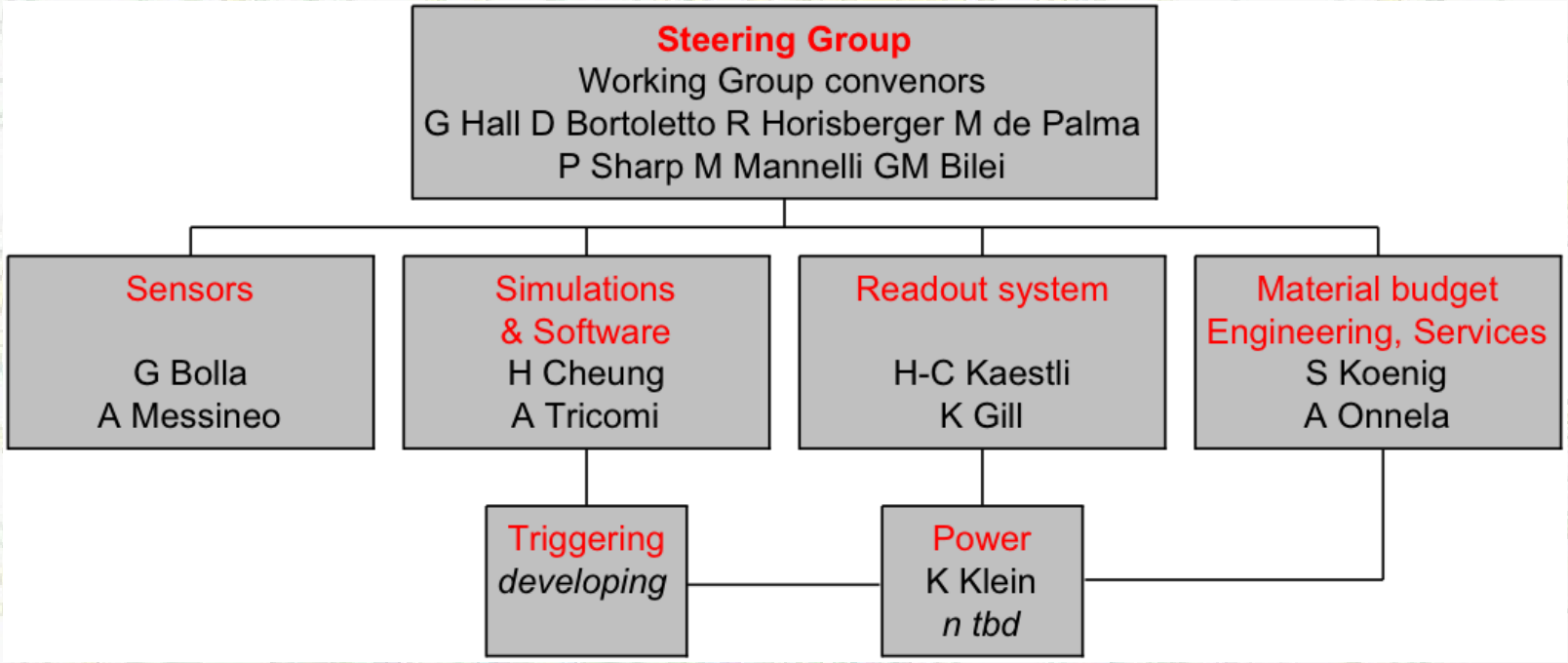
Year	Peak Lumi (x 10^{34})	Annual Integrated (fb^{-1})	Total Integrated (fb^{-1})
2009	0.1	6	6
2010	0.2	12	18
2011	0.5	30	48
2012	1	60	108
2013	1.5	90	198
2014	2	120	318
2015	2.5	150	468
2016	3	180	648
2017	3	0	648
2018	5	300	948
2019	8	420	1428
2020	10	540	2028
2021	10	600	2628
2022	10	600	3228
2023	10	600	3828
2024	10	600	4428
2025	10	600	5028

Garoby LHCC July 1, 2008

CMS Planning for Upgrade Project

- The SLHC planning assumption
  - Phase I to 2 x 10^{34} around 2013
  - Phase II to 10^{35} incrementally from ~2017
- Developing and building a new tracker (for Phase II) requires ~10 years
  - 5 years R&D
  - 2 years Qualification
  - 3 years Construction
  - 6 months Installation and Ready for Commissioning
- NB – even this is aggressive
  - System design and attention to QA are important considerations from a very early stage
  - Cost was a driver for LHC detectors from day one

CMS Planning for Upgrade Project

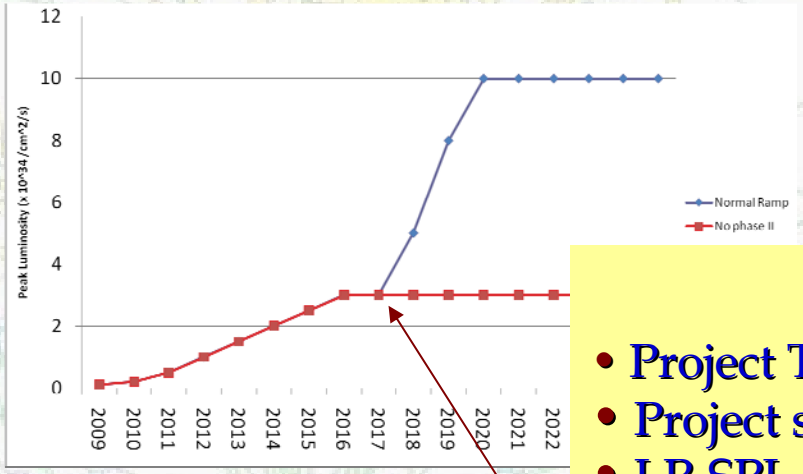


Phase I Upgrades

Phase II Upgrades

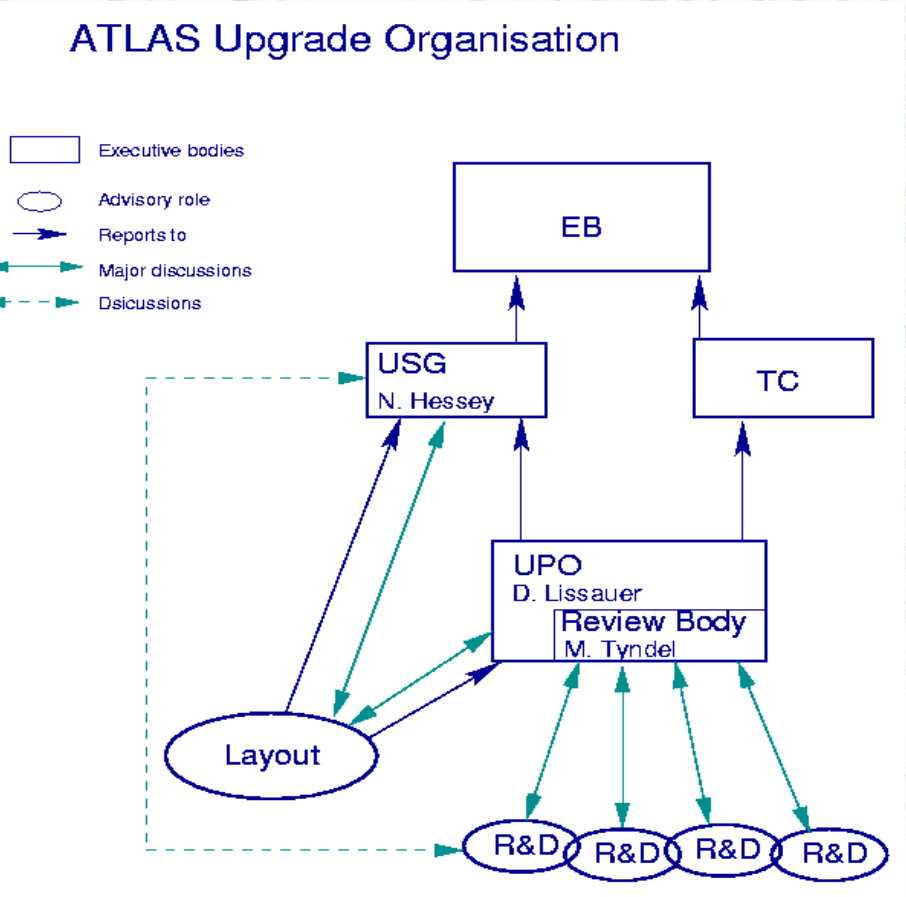
ATLAS Planning for Upgrade Project

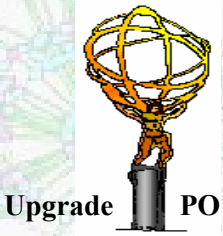
After collaboration meetings and workshops at Genoa, Liverpool and Valencia, the ATLAS Collaboration has defined a programme for the Luminosity Upgraded LHC.



Milestones

- Project TDR: June 2011
- Project start: January 2012
- LP-SPL commissioning: mid-2015
- PS2 commissioning: mid-2016
- SPS commissioning: May 2017
- Beam for physics: July 2017





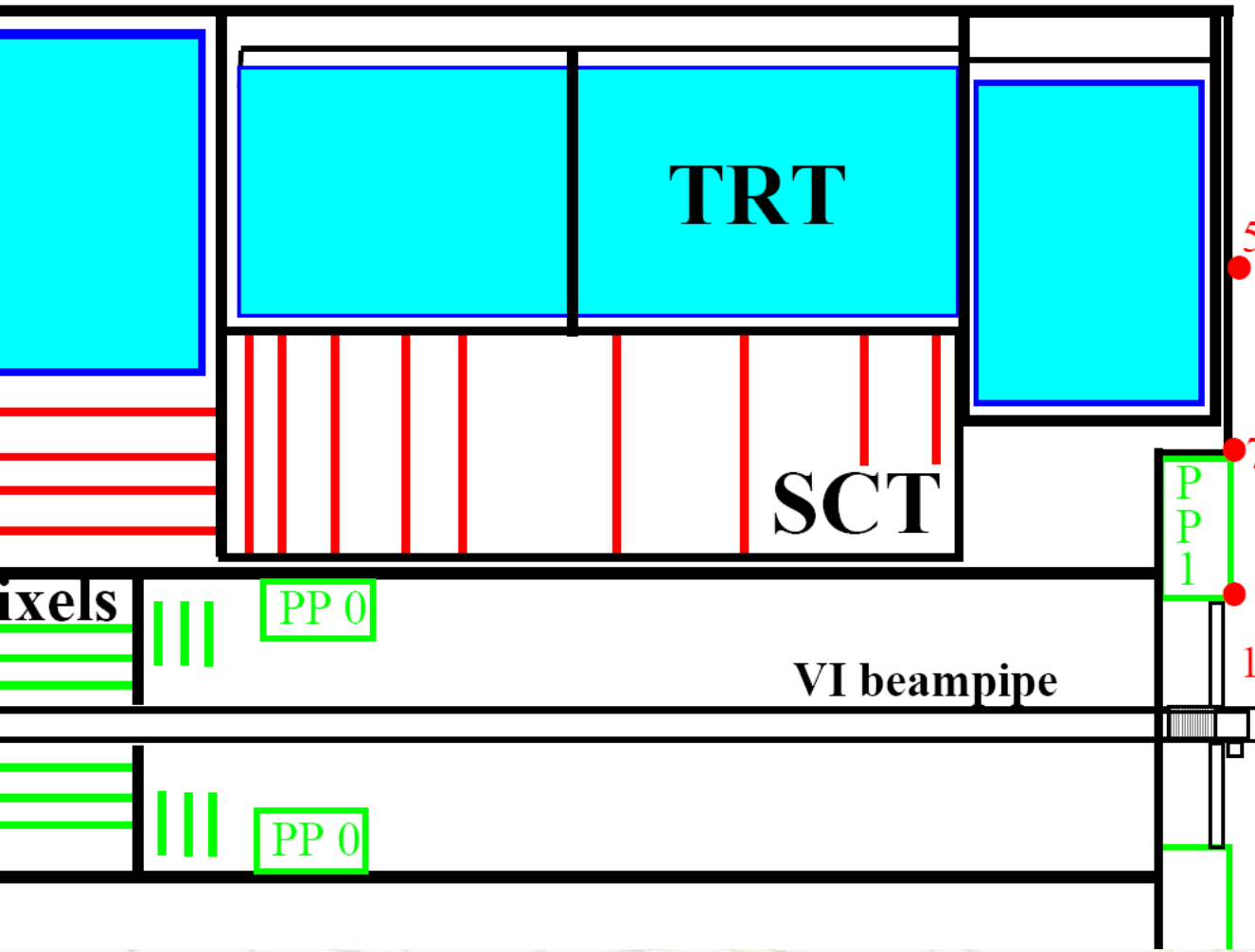
ATLAS has defined an overall management structure for the Upgrade programme with an Upgrade Steering Group answering directly to the ATLAS Executive Board and sitting at the same level as ATLAS Technical Coordination. Below this sits the Upgrade Project Office with individual research ad development programmes reporting to it.

LAr Calorimeter

Dose rates after 10 years of running and 30 days of cooling.

Requirements to reuse much of ATLAS (including services) and the levels of activation anticipated, greatly complicate upgrade tracker installation

(Existing tracker cables only rated to 500V but replacement would require dismantling of significant parts of the muon system)

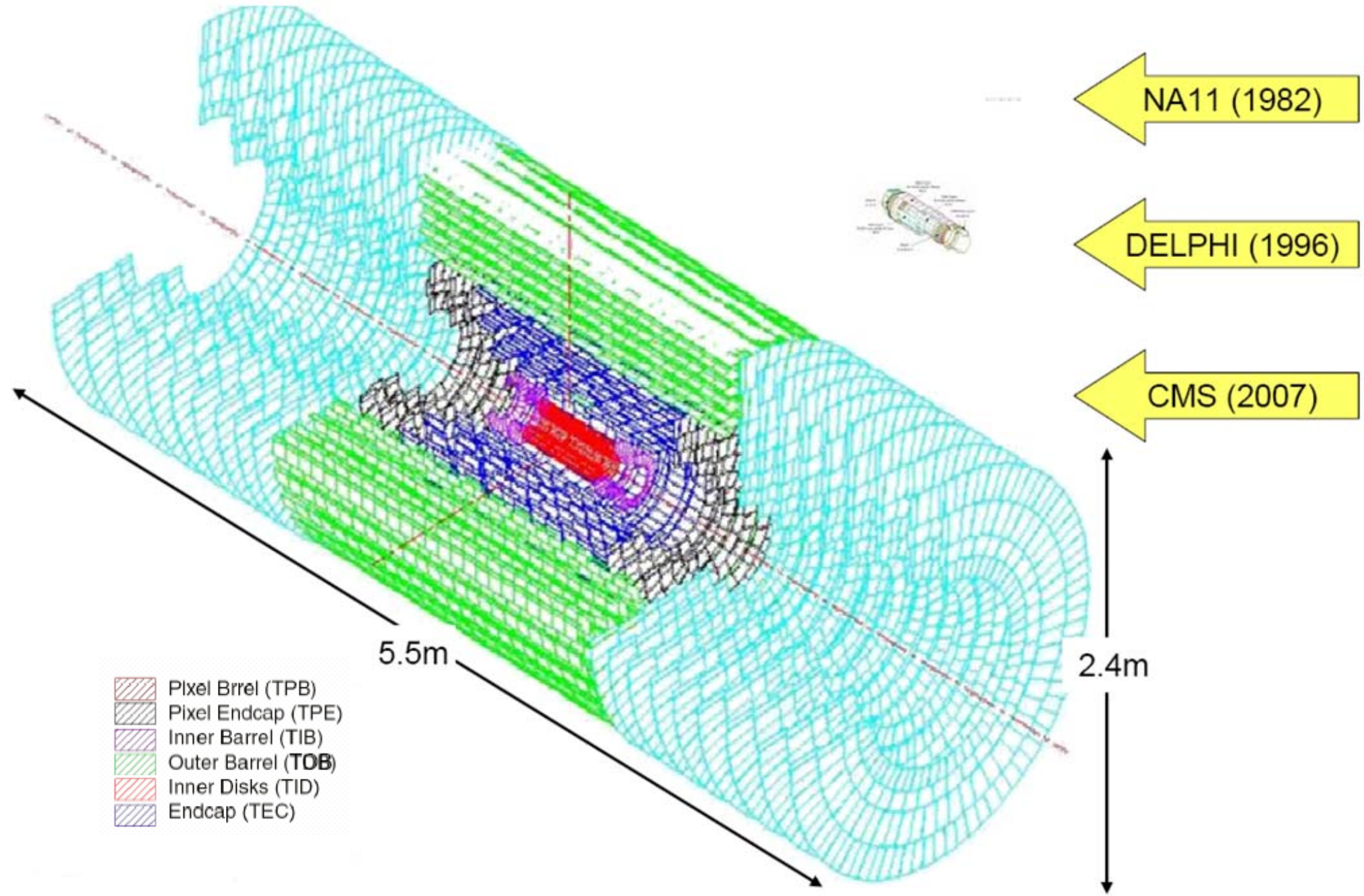


	Pixels	SCT	TRT	LAr	VI
58 μSv/h:	37	8	4	8	1
Neut. act.:	29%	42%	29%	23%	0%
Services:	78%	86%	64%		

	Pixels	SCT	TRT	LAr	VI
73 μSv/h:	51	8	3	8	3
Neut. act.:	18%	41%	30%	25%	0%
Services:	59%	84%	63%		

	Pixels	SCT	TRT	LAr	VI
144μSv/h:	118	9	3	8	6
Neut. act.:	4%	41%	30%	25%	0%
Services:	9%	82%	62%		

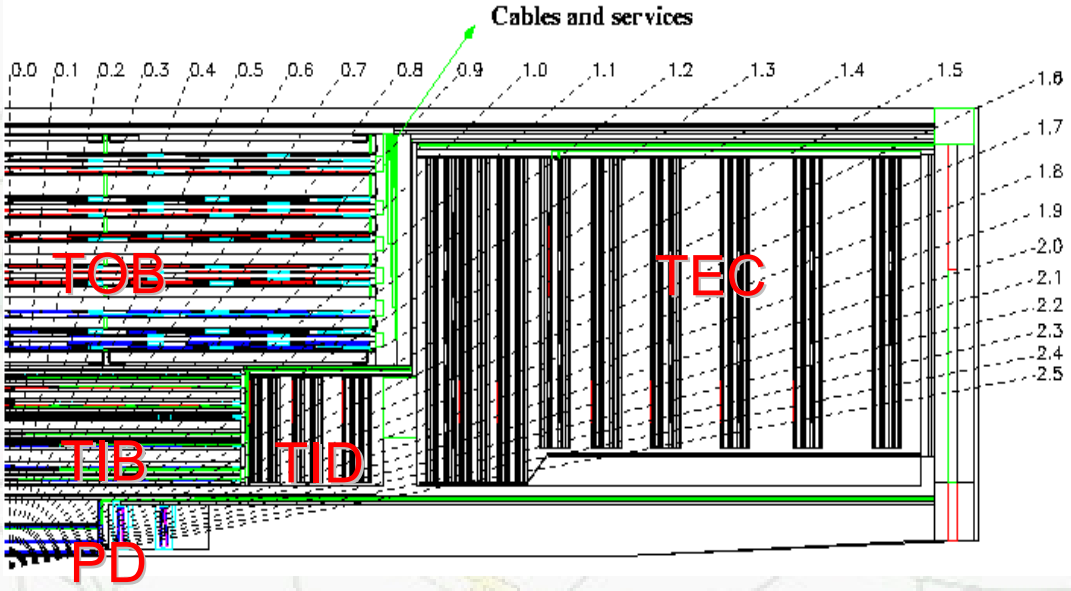
CMS Silicon Tracker Largest Ever Built

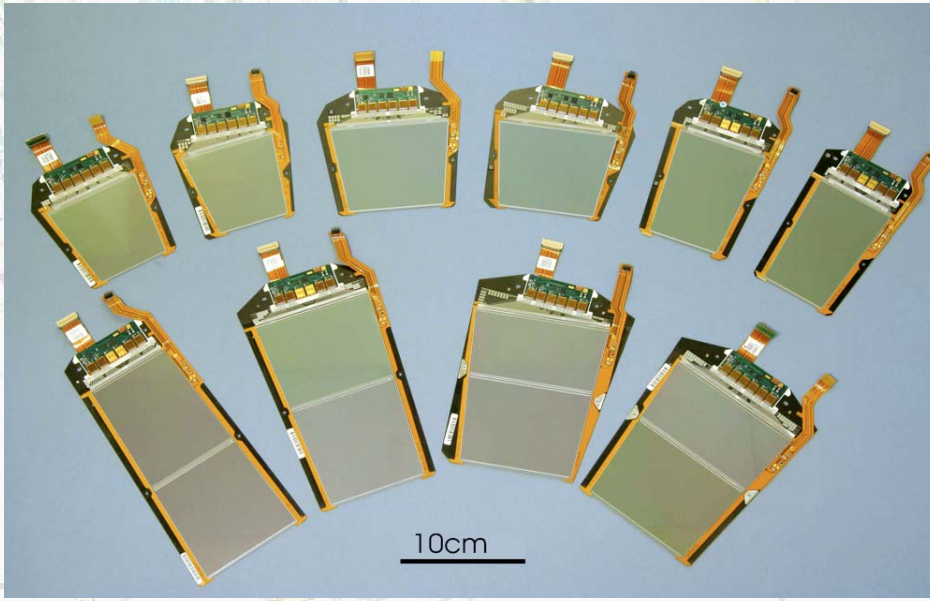


Current CMS Tracker System

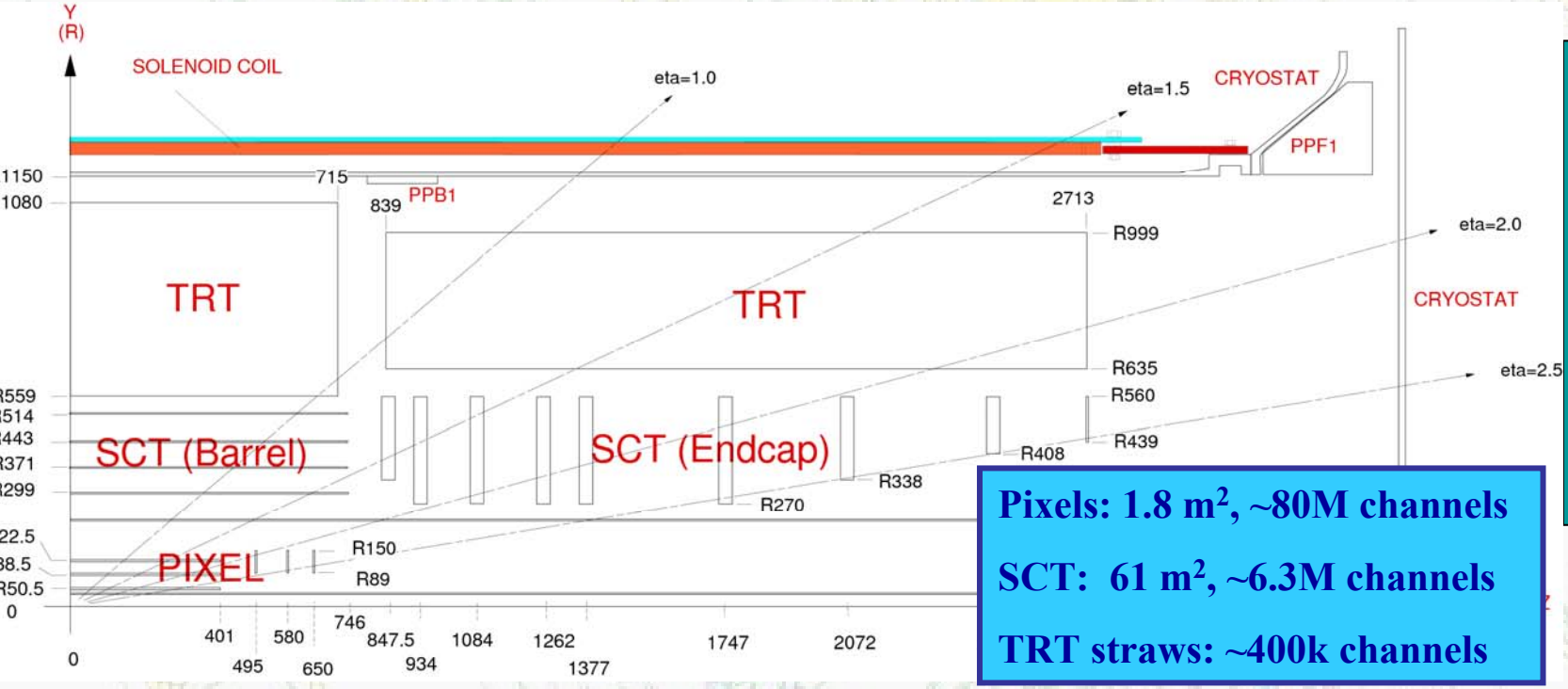
- Two main sub-systems: Silicon Strip Tracker and Pixels
  - pixels quickly removable for beam-pipe bake-out or replacement

Microstrip tracker	Pixels
~210 m^2 of silicon, 9.3M channels	~1 m^2 of silicon, 66M channels
73k APV25s, 38k optical links, 440 FEDs	16k ROCs, 2k olinks, 40 FEDs
27 module types	8 module types
~34kW	~3.6kW (post-rad)





Current ATLAS Inner Tracker Layout

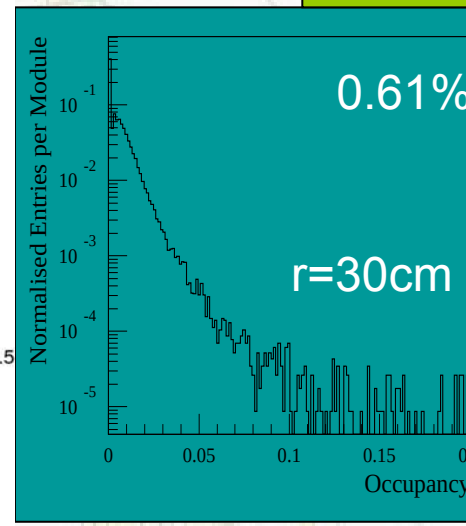


Pixels: 1.8 m², ~80M channels

SCT: 61 m², ~6.3M channels

TRT straws: ~400k channels

ID TDR



Mean Occupancy in Innermost Layer of Current SCT

xels (50 μm × 400 μm): 3 barrels, 2×3 disks — 5cm < r < 15cm

Pattern recognition in high occupancy region

mpact parameter resolution (in 3d)

adiation hard technology: n^+-in-n Silicon technology, operated at -6°C

rips (80 μm × 12 cm) (small stereo angle): "SCT" 4 barrels, 2×9 disks

pattern recognition — 30cm < r < 51cm

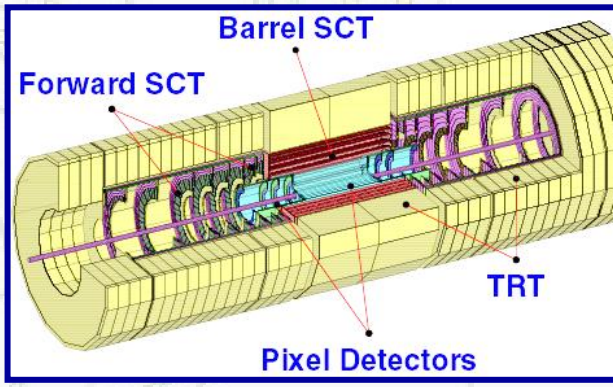
momentum resolution

strips in n-type silicon, operated at -7°C

RT 4mm diameter straw drift tubes: barrel + wheels — 55cm < r < 105cm

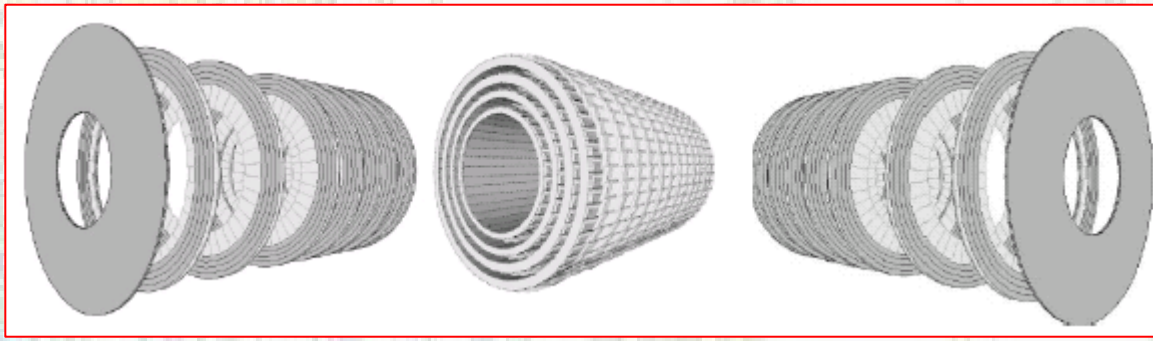
Additional pattern recognition by having many hits (~36)

Standalone electron id. from transition radiation

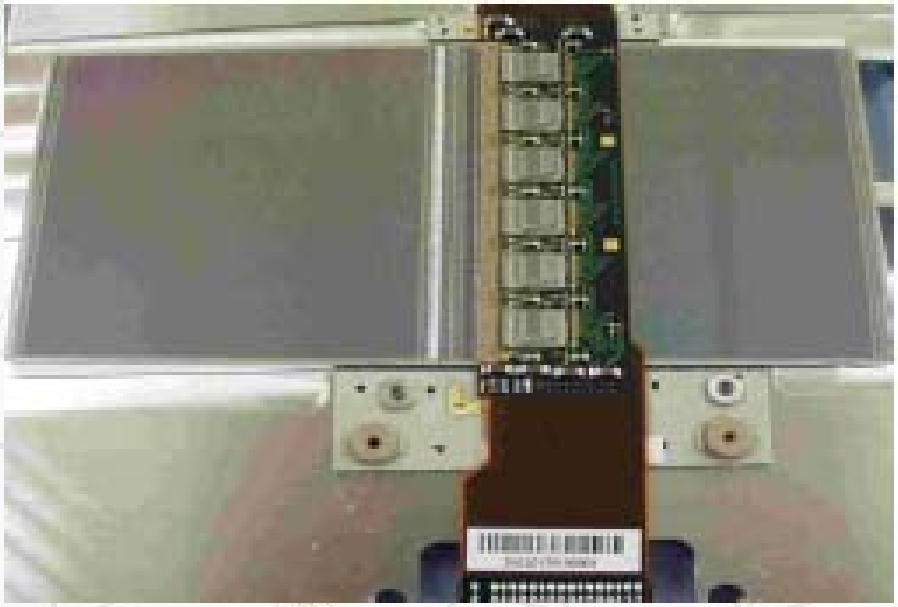


Current SCT ATLAS Module Designs

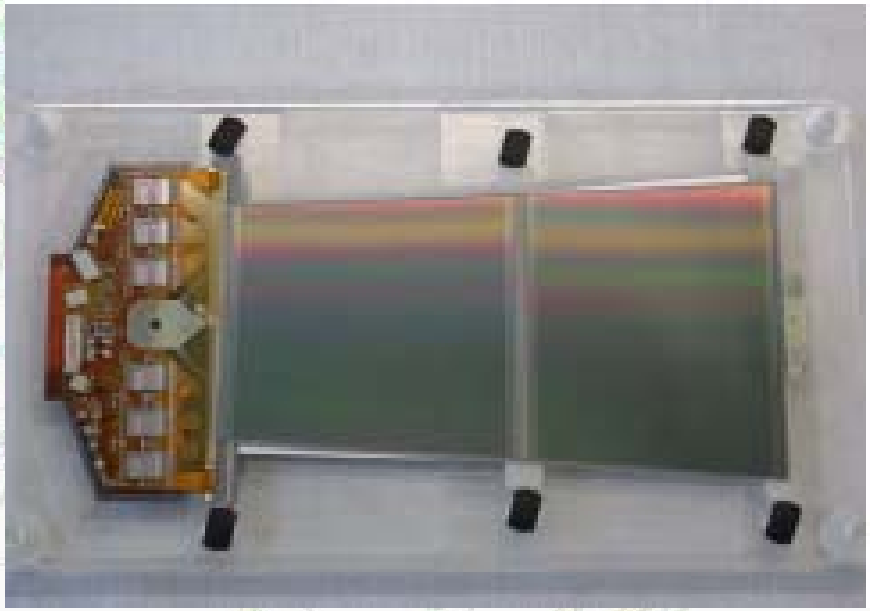
ATLAS Tracker Based on Barrel and Disc Supports



Effectively two styles of double-sided modules (2×6cm long

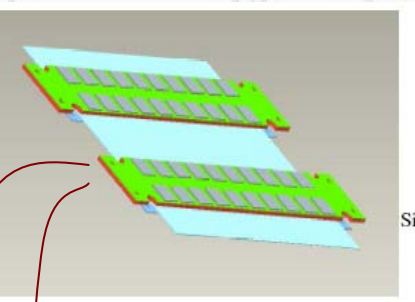


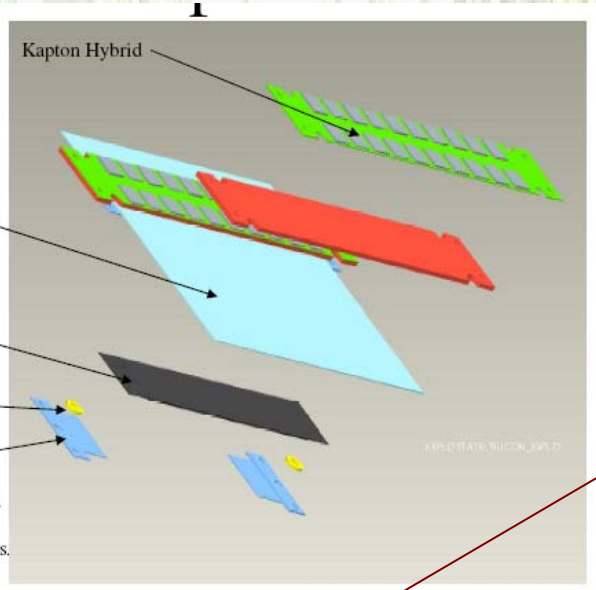
Barrel Modules
(Hybrid bridge above sensors)



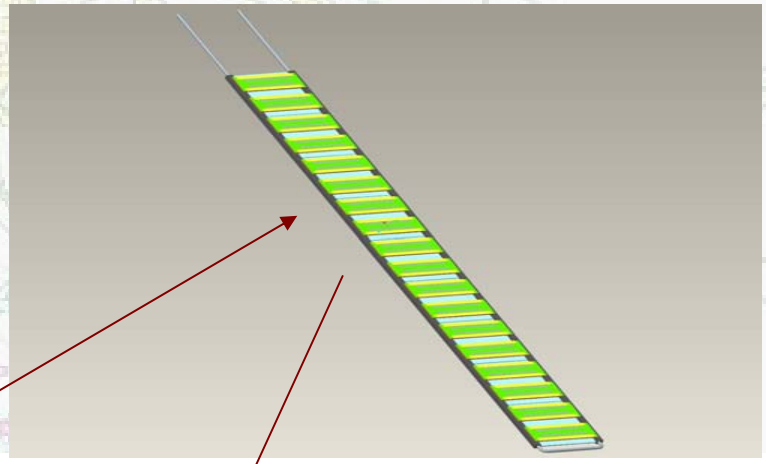
Forward Modules
(Hybrid at module end)

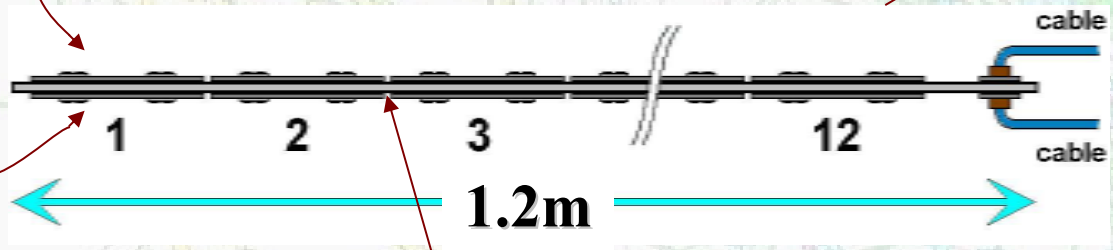
ATLAS Tracker Upgrade Module Concep

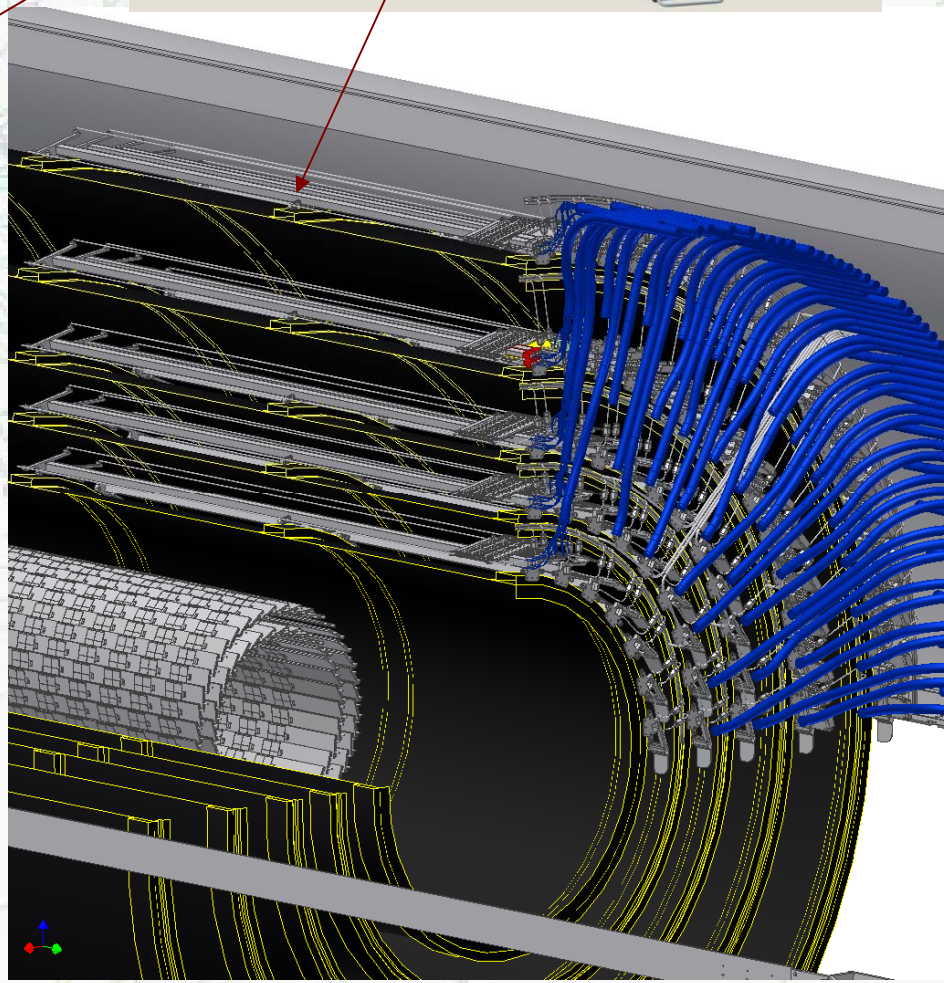


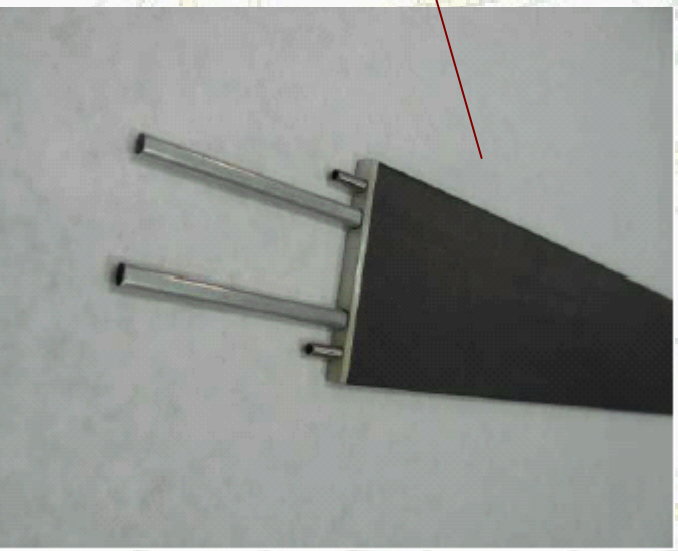


Single sided silicon module.
Alumina and TPG heat spreader, spliced as in ATLAS module.
Integral precision location washers (holes and slots)
Carbon Carbon hybrid base, with added non conductive spacers.





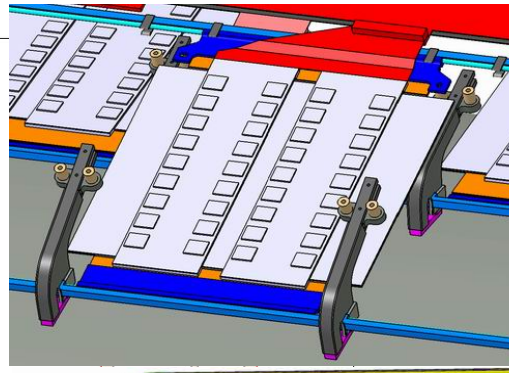


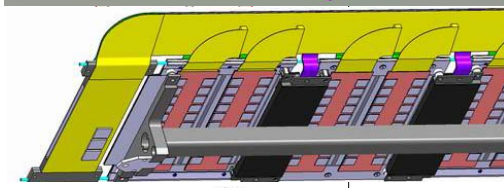


Double-sided Module Option

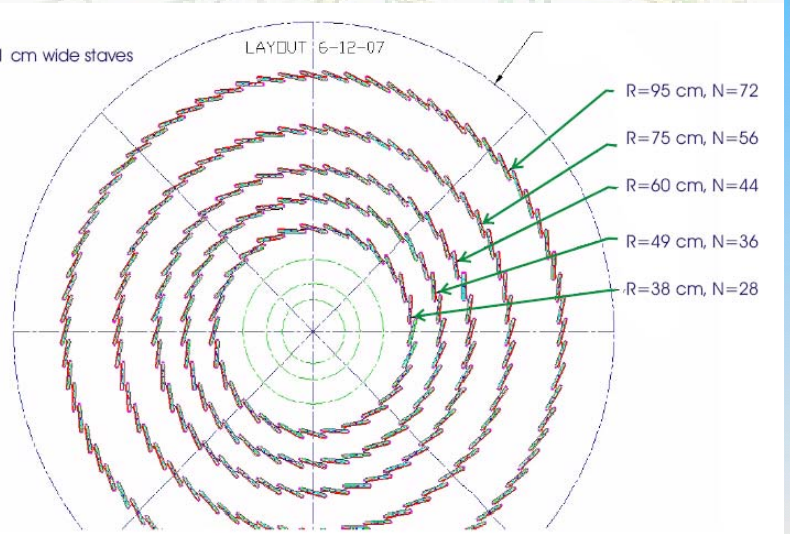
- Chip size 0.3mm x 7.5mm x 7.2mm
- Width of Hybrid 25mm

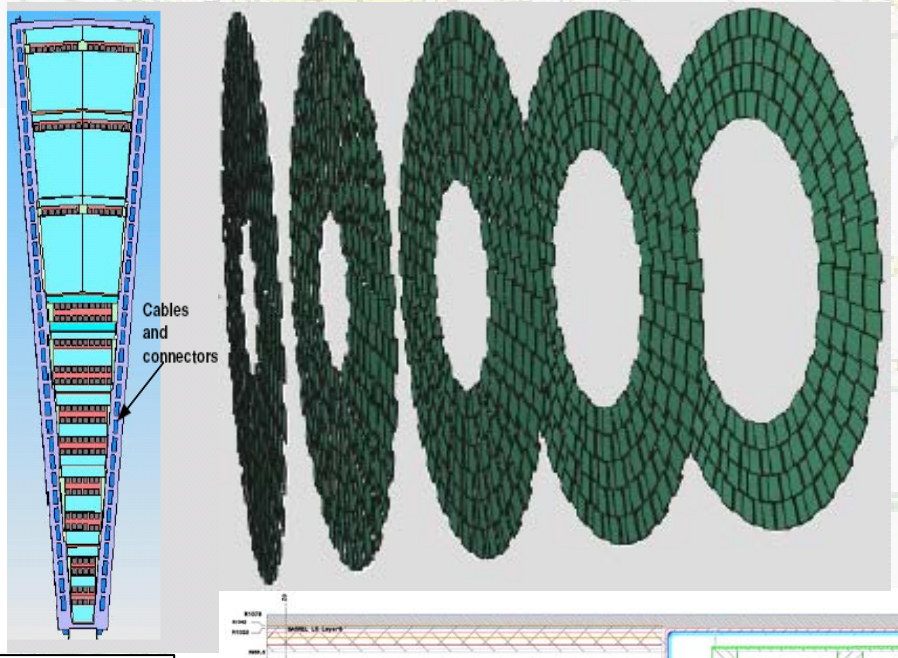
Y. Unno (KEK)

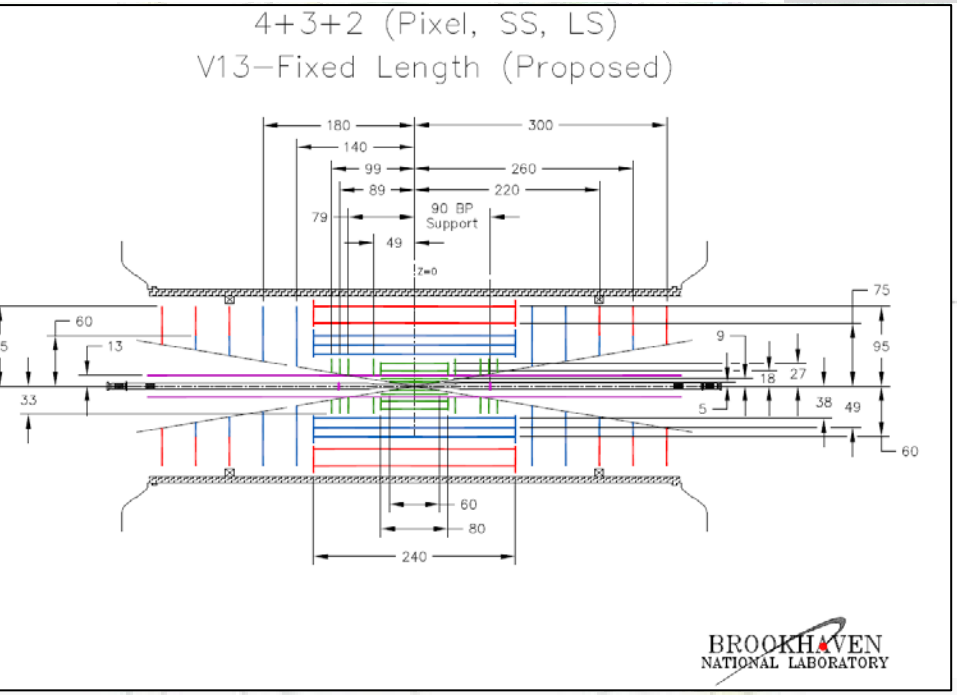


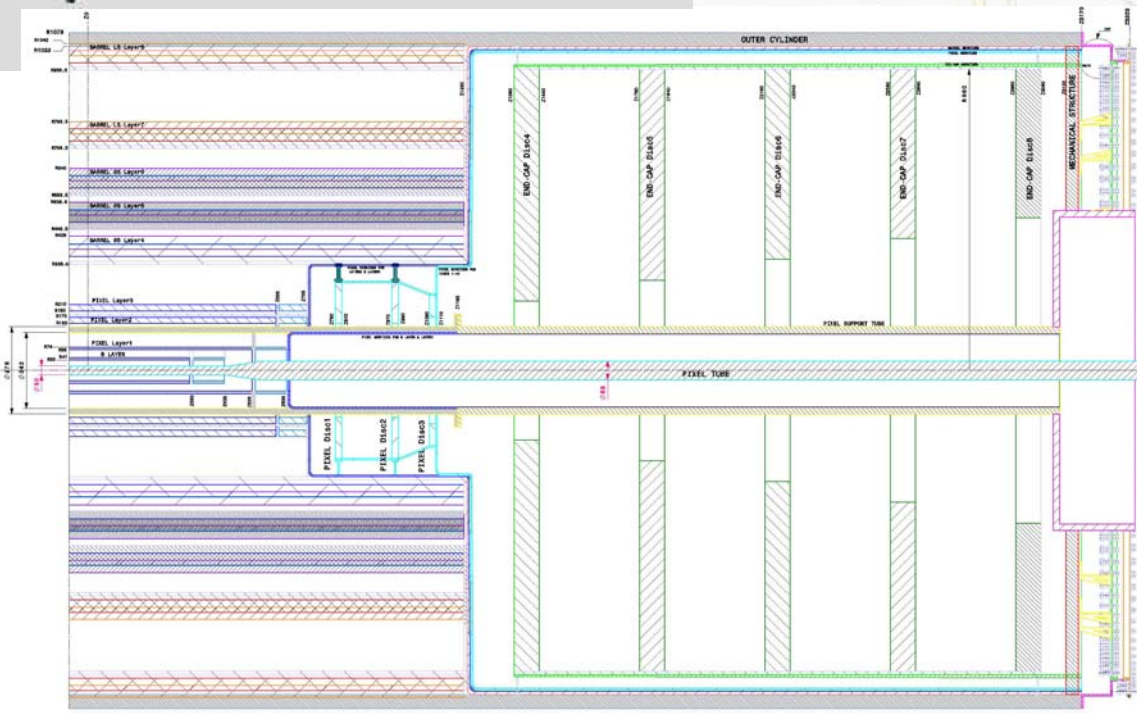


ATLAS Tracker Upgrade Layout





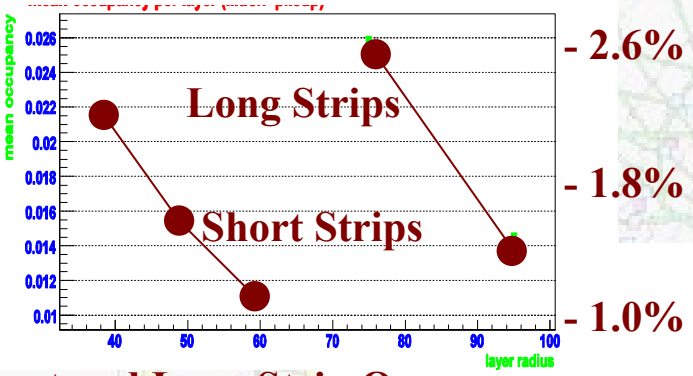




ATLAS SLHC Tracker Layout Simulation

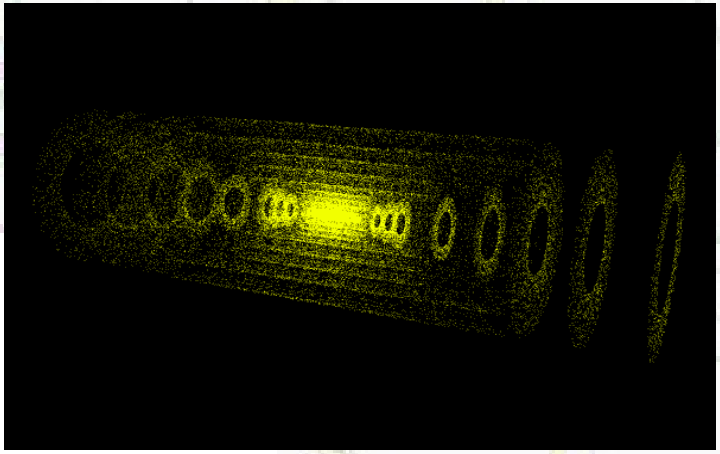
Strawman-08 4+3+2

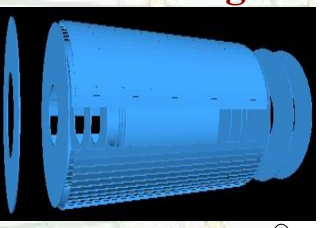
Pixel Tracker Layers:	**r = 3–5cm, 12cm, 18cm, 27cm**	**z = ±40cm**
Short Strip (2.4 cm) μ-strips (stereo layers):	**r = 38cm, 49cm, 60cm**	**z = ±120cm**
Long Strip (9.6 cm) μ-strips (stereo layers):	**r = 75cm, 95cm**	**z = ±120cm**

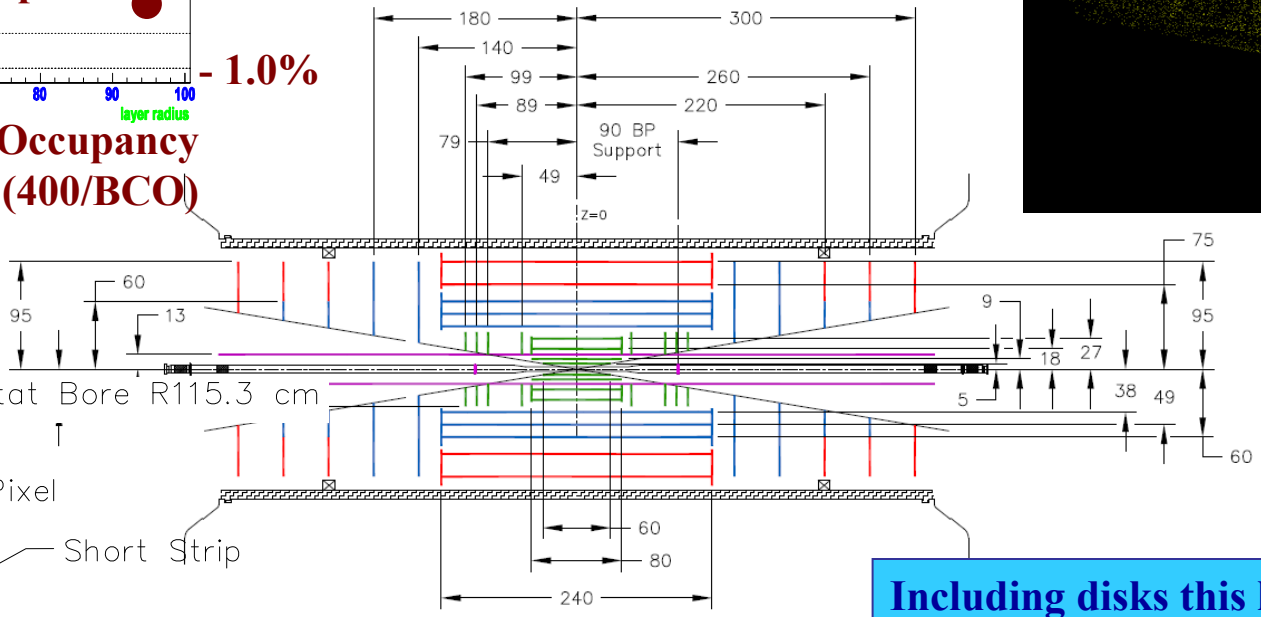


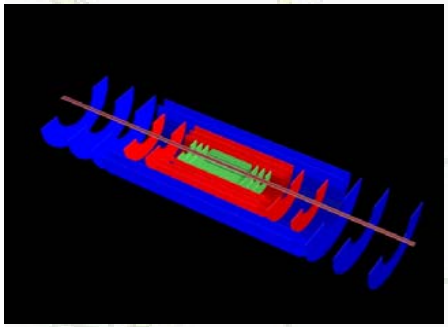
ort and Long Strip Occupancy (400/BCO)

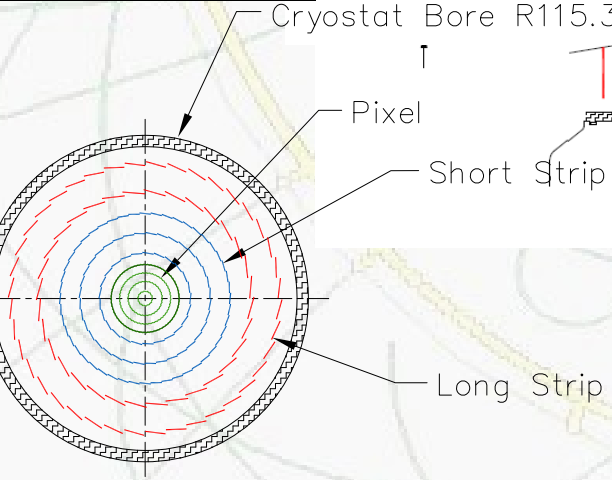
Only LO MC (Pythia) . May need to include ×2 safety factor? Occupancy estimates already worryingly high…











Material target is for 3 layer inner barrel to match current 4 layer SCT

Including disks this leads to:

Pixels: 5-10 m², ~500,000,000 channels

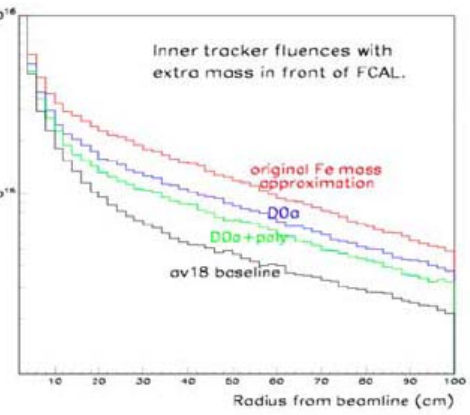
Short strips: 60 m², ~30,000,000 channels

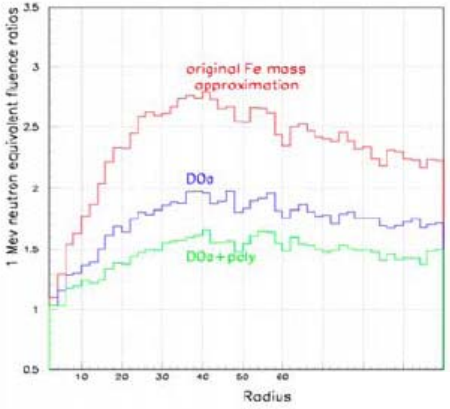
Long strips: 100 m², ~15,000,000 channels

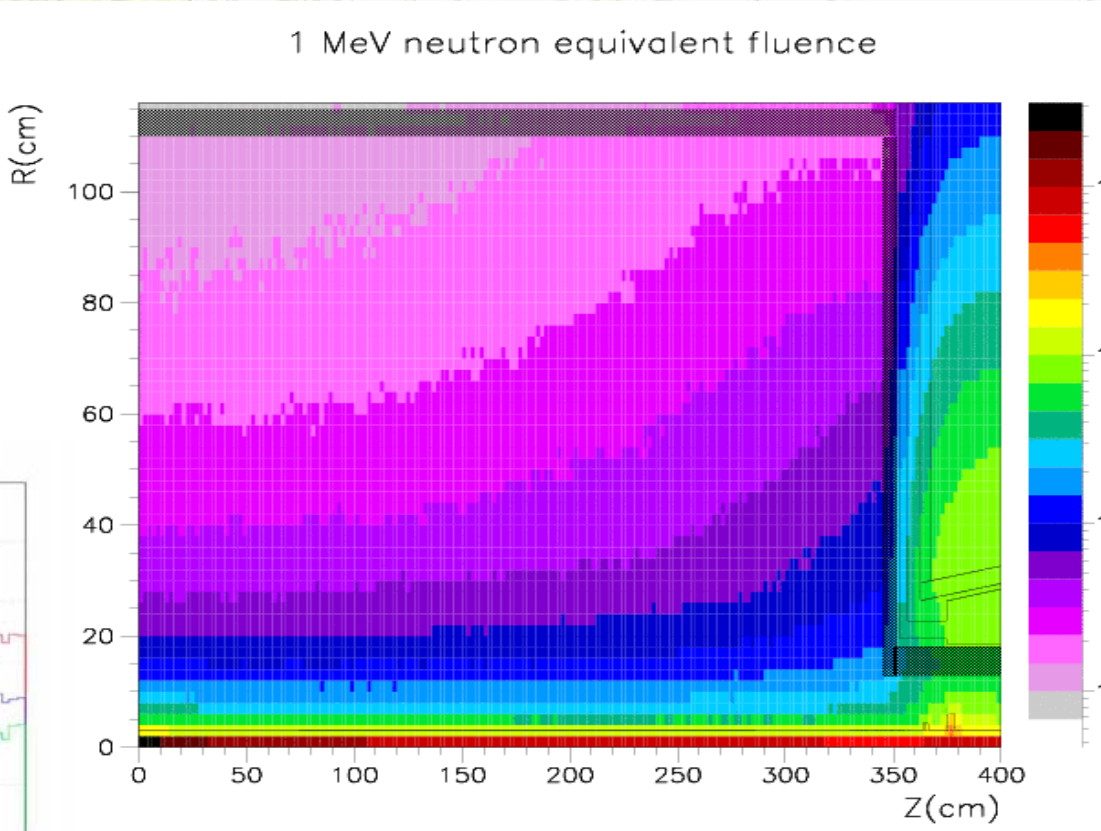
ATLAS Radiation Fluence Simulation

FLUKA2006 Monte Carlo used to set detector radiation hardness requirements and define moderator design

Also to achieve full luminosity, additional magnets may need to be placed within the experiment.



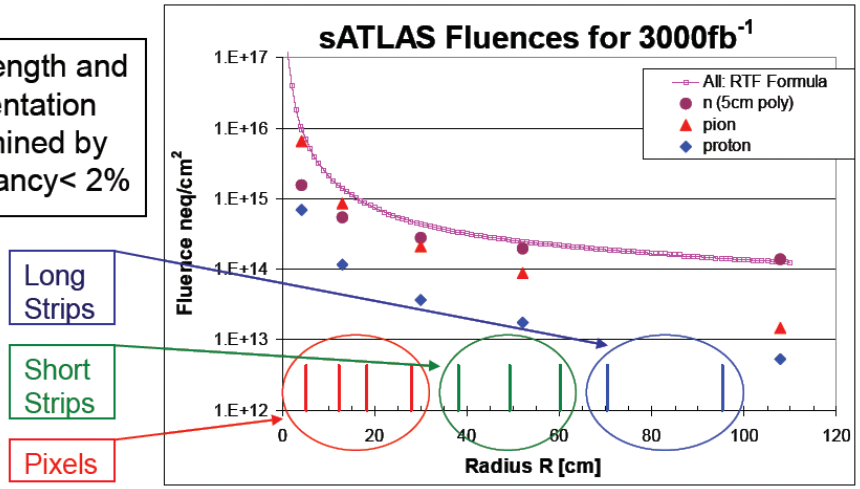




Implications studied for radiation field could be ×2 without extra moderator

A major requirement for progress is cross-checking with dose measurements once the LHC starts, and then retuning the models

Strip length and segmentation determined by occupancy< 2%



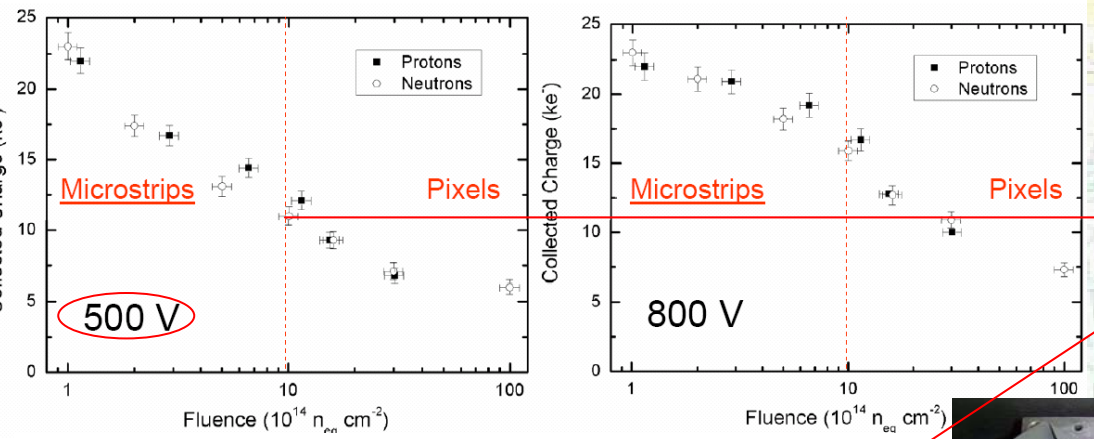
ATLAS Radiation Taskforce http://atlas.web.cern.ch/Atlas/GROUPS/PHYSICS/RADIATION/RadiationTF_document.html

Mix of neutrons, protons, pions depending on radius R

Long and short strips damage largely due to neutrons

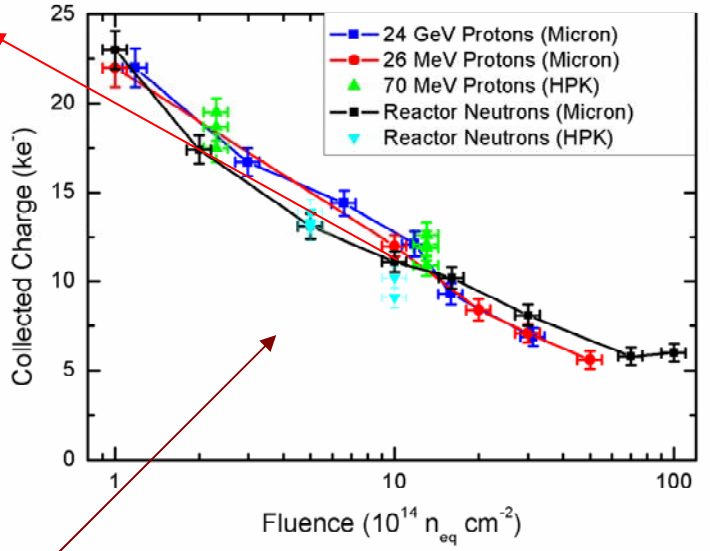
Pixels damage due to neutrons and pions

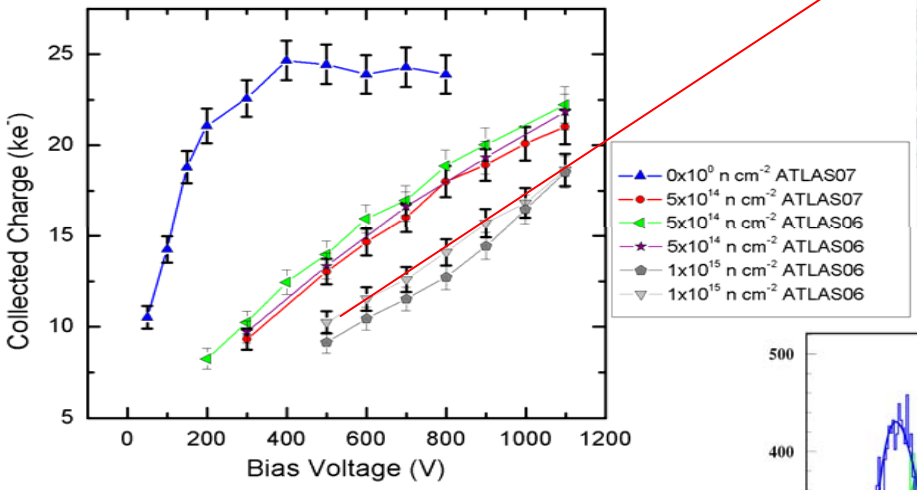
ATLAS Microstrip Sensor Radiation Studie



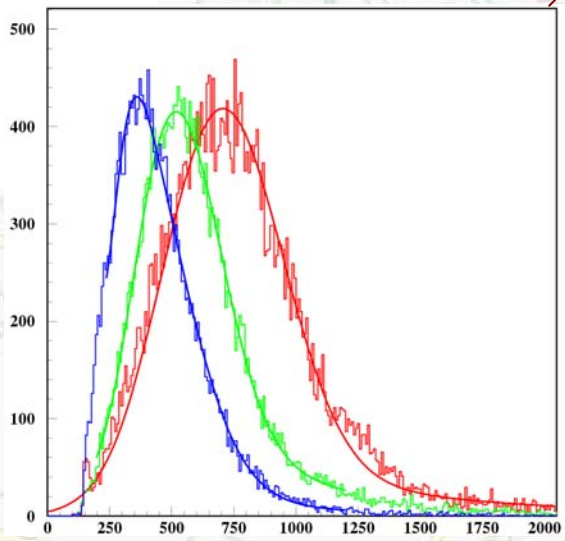
New trackers required to survive 6000fb^{-1} ie short strip detectors to withstand $9\times10^{14}n_{eq}/cm^2$ (50% neutrons) at 500V

With 750e$^-$ noise, ⟶ expect S/N ≈12-15



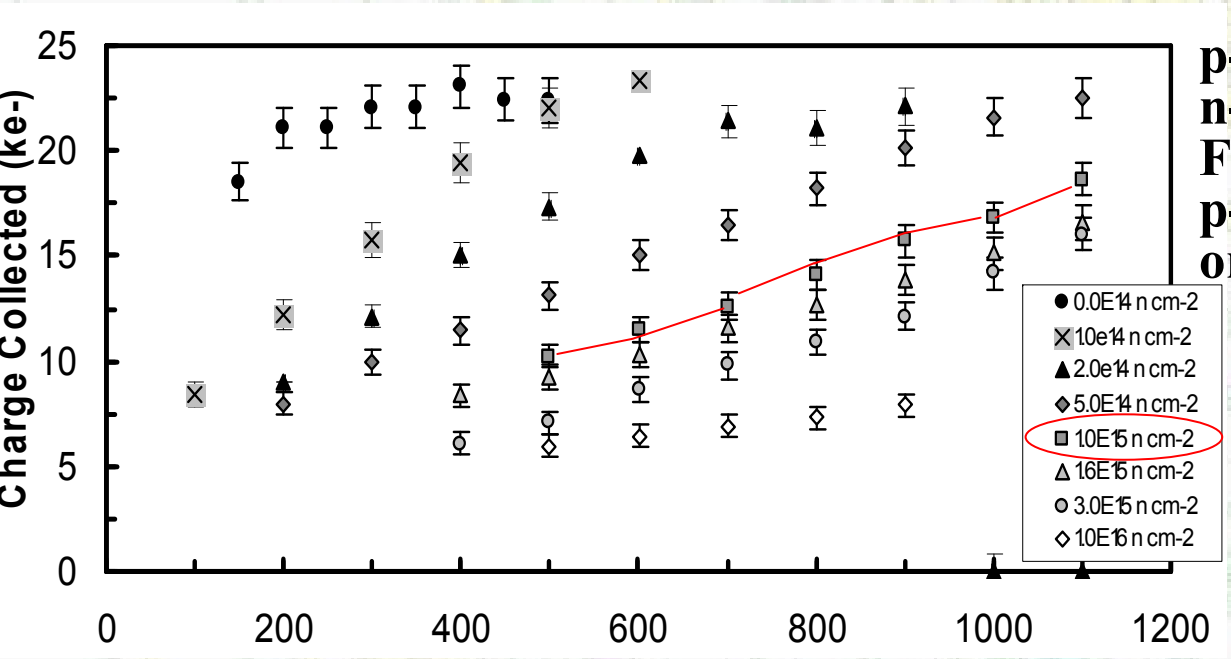


Minimum Ionising Particle (m.i.p.) Charge Collection Efficiency CCE (V) Planar p-type Hamamatsu Doses to $10^{15}n_{eq}/cm^2$ (Ljubljana reactor neutrons)

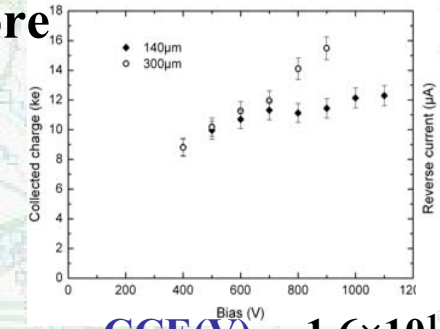


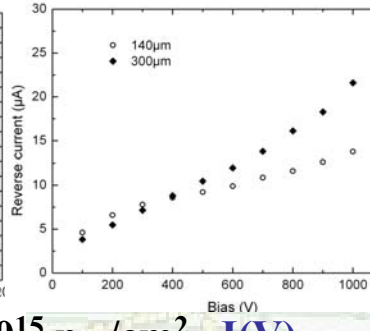
m.i.p. CCE at 500V for planar p-type miniature sensors from different manufacturers and irradiation species, normalised by non-ionising energy loss (NIEL) doses up to $10^{16}n_{eq}/cm^2$

ATLAS Microstrip Sensor Radiation Studie



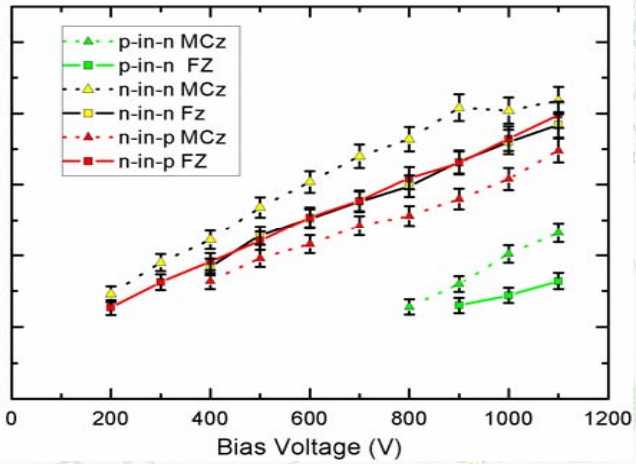
p-in-n not useable above ~5×10^{14}n/cm^2
n-in-n MCz slightly better than n-in-n FZ or n-in-p (either MCz or FZ)
p-in-n FZ looks useable even to 10^{16}n/cm^2 or more

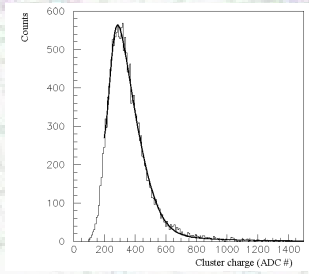




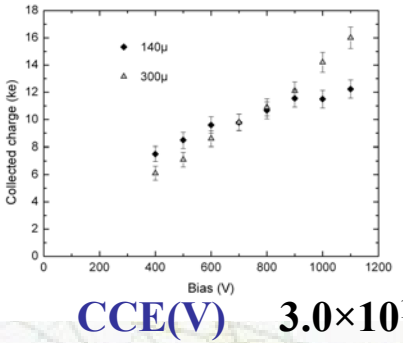
CCE(V) **1.6×10^{15} n$_{eq}$/cm^2** **I(V)**

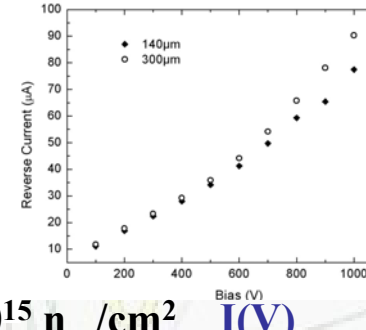
n.i.p. CCE (V) planar
neutron irradiated p-type



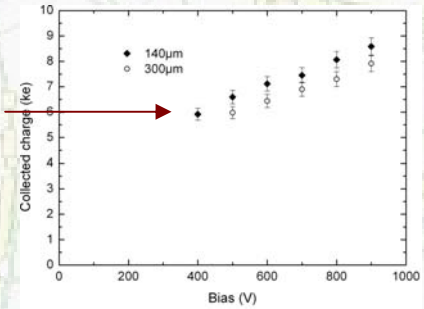


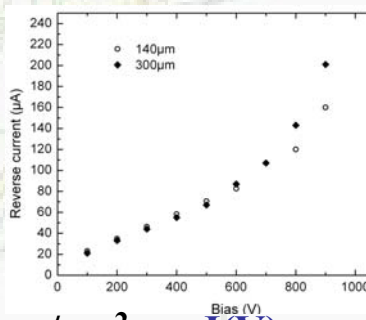
m.i.p. CCE (V)
Micron RD50
planar P-type
140µm and 300µm thickness
Doses up to 10^{16}n$_{eq}$/cm^2
(Ljubljana reactor neutrons)





CCE(V) **3.0×10^{15} n$_{eq}$/cm^2** **I(V)**





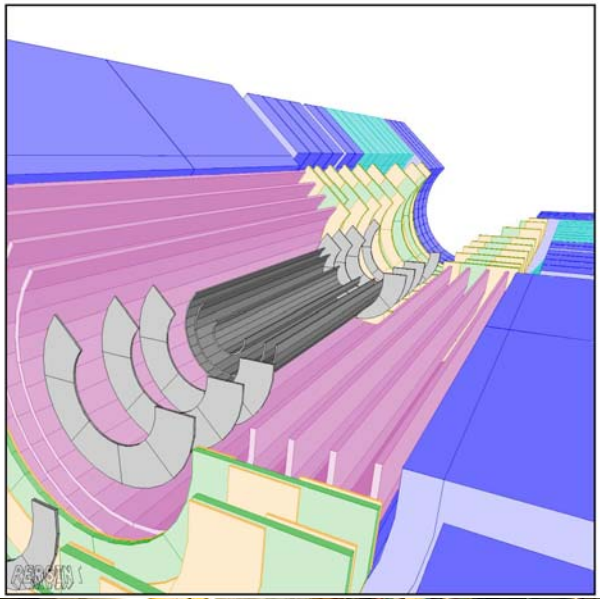
CCE(V) **10^{16} n$_{eq}$/cm^2** **I(V)**

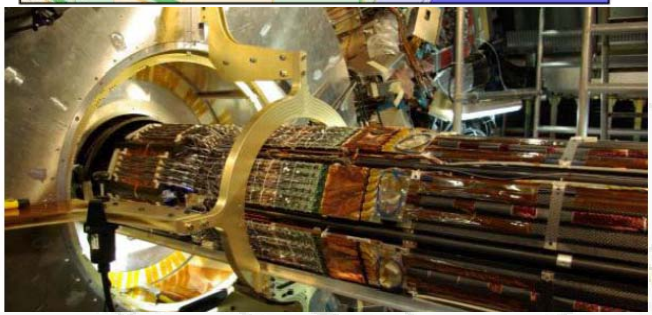
CCE (V) planar n-type and p-type Micron miniatures
after 10^{15}n/cm^2 (Ljubljana reactor neutrons) **No advantage in signal(V) or I(V) in using thin senso**

Vertex Detectors at Current LHC

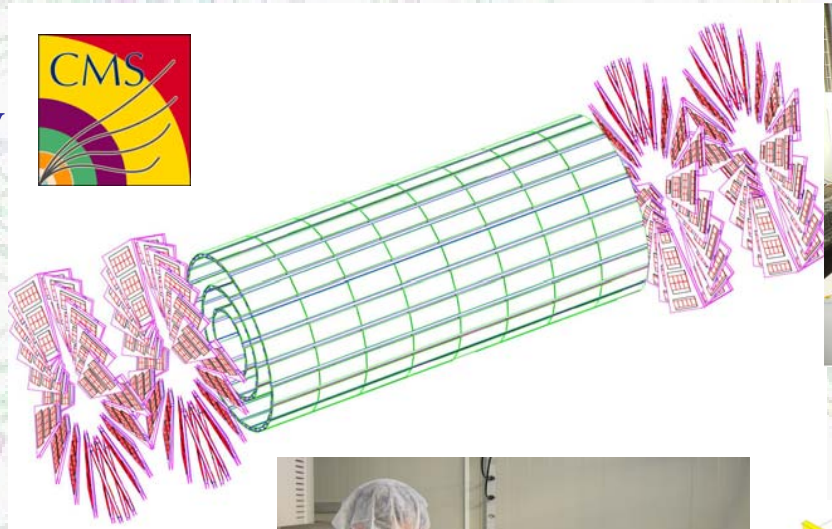
LHC vertex detectors all use n^+ implants in n^- bulk:

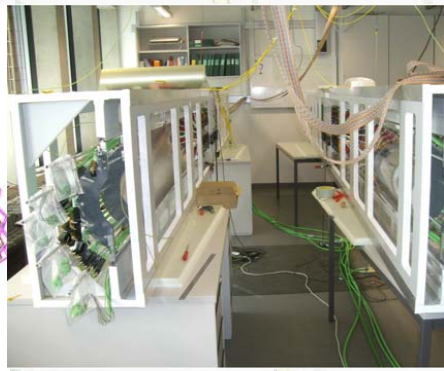
- **Because of advantages after heavy irradiation from collecting electrons on n^+ implants, the detectors at the LHC (ATLAS and CMS Pixels and LHCb Vertex Locator) have all adopted the n^+ in n^- configuration for doses of $5 - 10 \times 10^{14}$ $n_{eq}cm^{-2}$**
- **Requires 2-sided lithography**



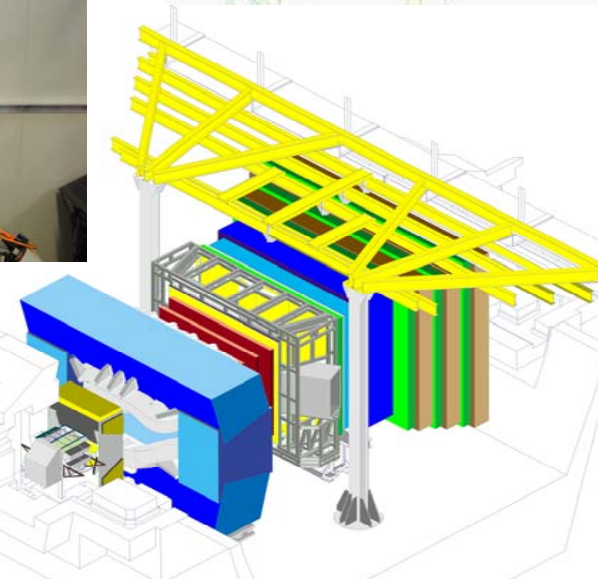


ATLAS 100 million Pixels





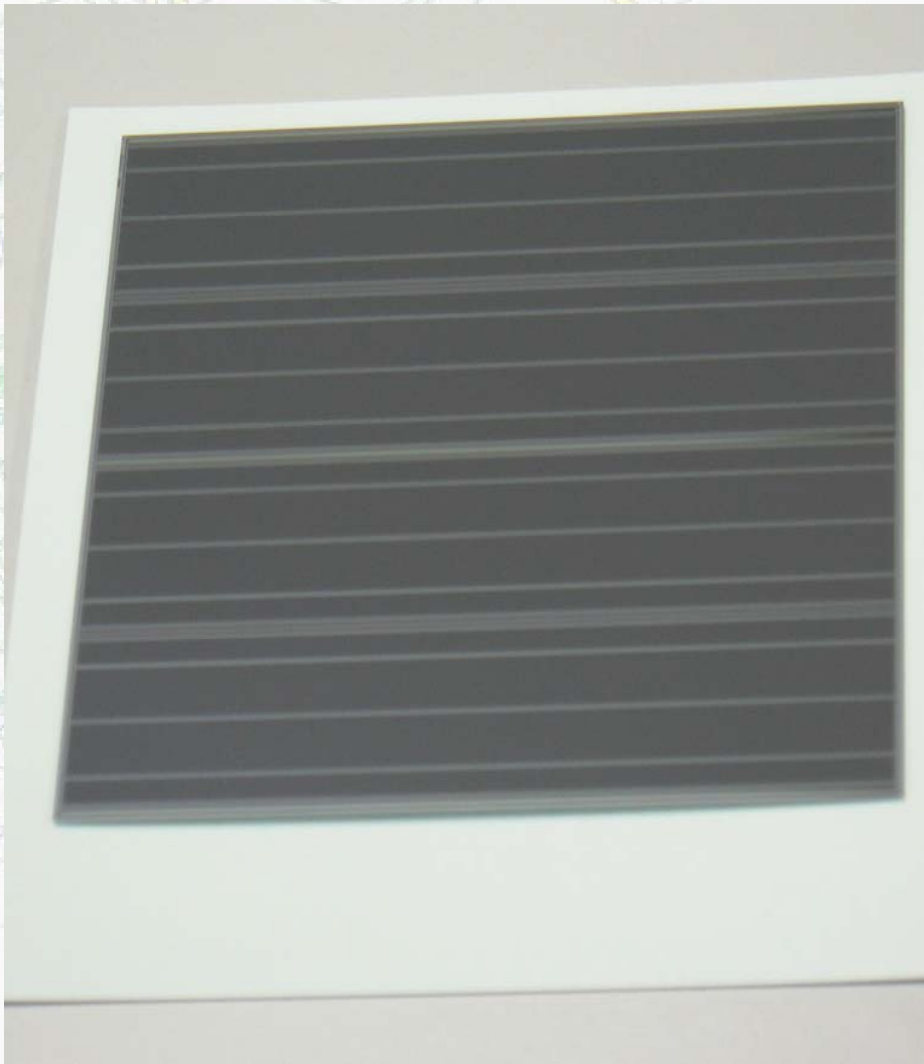
LHCb
Vertex Locator
Z(mm)=0-990



Motivations for P-type

Starting with a p^--type substrate offers the advantages of single-sided processing while keeping n^+-side read-out:

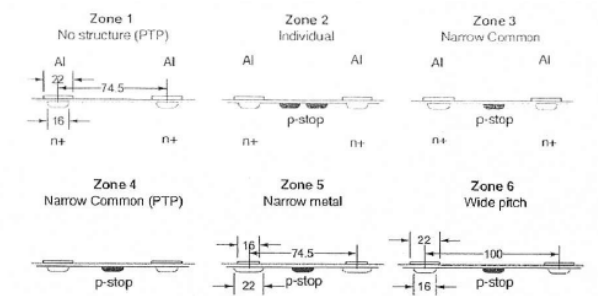
- **Processing Costs (~50% cheaper).**
- **Greater potential choice of suppliers.**
- **High fields always on the same side.**
- **Easy of handling during testing.**
- **No delicate back-side implanted structures to be considered in module design or mechanical assembly.**

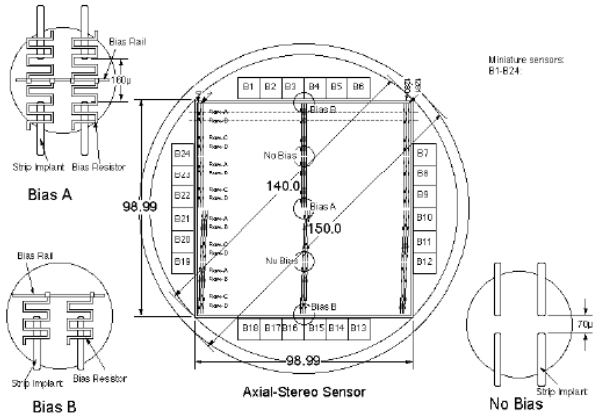


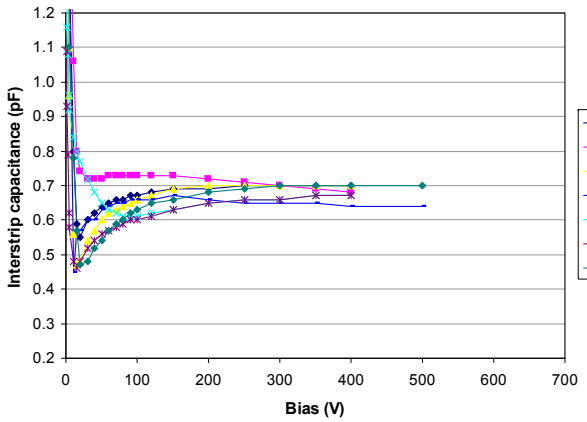
So far, capacitively coupled, polysilicon biased p-type devices fabricated to ATLAS provided mask designs by:

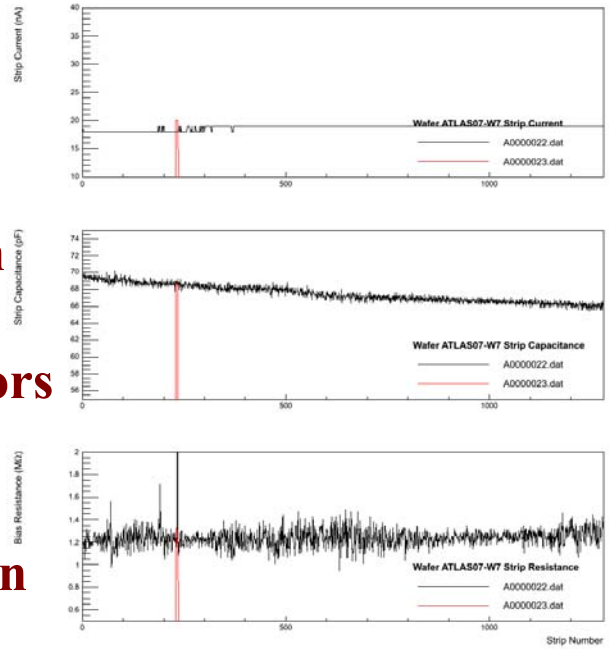
- **Micron Semiconductor (UK) Ltd (existing ATLAS barrel: 6cm×6cm and RD50 miniatures: 1cm ×1cm),**
- **CNM Barcelona (RD50 miniatures: 1cm×1cm),**
- **ITC Trento (RD50 miniatures: 1cm×1cm)**
- **Hamamatsu Photonics HPK (1cm×1cm and 10cm×10cm Full ATLAS prototypes)**

Microstrip Sensor Testing

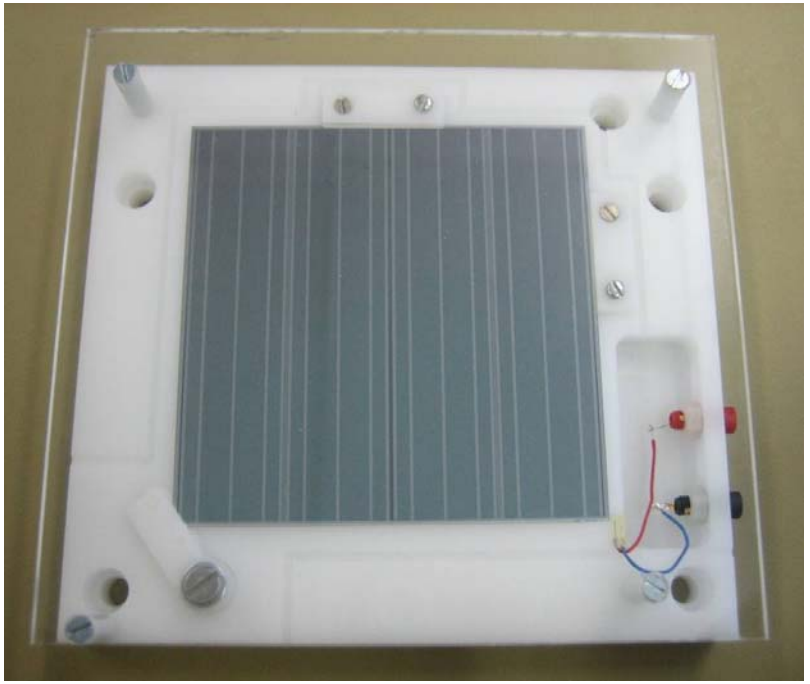








Interstrip resistance, capacitance and breakdown characteristics have been studies on miniature detectors representing 6 different detailed designs for the n-implant interstrip isolation



3 large area sensors have been delivered to and all 5120 strips capacitors tested to 100V
→ Total strip yield >99%

Each sensor has 4 rows for 1280 strips at 74.5µm pitch

3 different processing runs are ordered with p-spray only, p-implant only and both as n-strip isolation technologies

ATLAS Microstrip ASIC Design

Front-End	Optimised for short strip but power tuning capability for long strips	27mA/chip (tuneable) ✓ 750enc (2.5cm strips) Final S/N > 10 ✓
Back-End	Main change in DCL block to 80MHz	92-96mA/chip at 2.5V nominal
Powering	2 integrated shunt regulators schemes	Current limiting option to impose uniformity
Floor Plan	Width to allow direct bonding to sensors	7.5mm by 7.7mm
Data Buffering	Pipeline and derandomizer implemented	
Submission	June 2008 (IBM 0.25μm)	**Just delivered, and diced chips due this week**

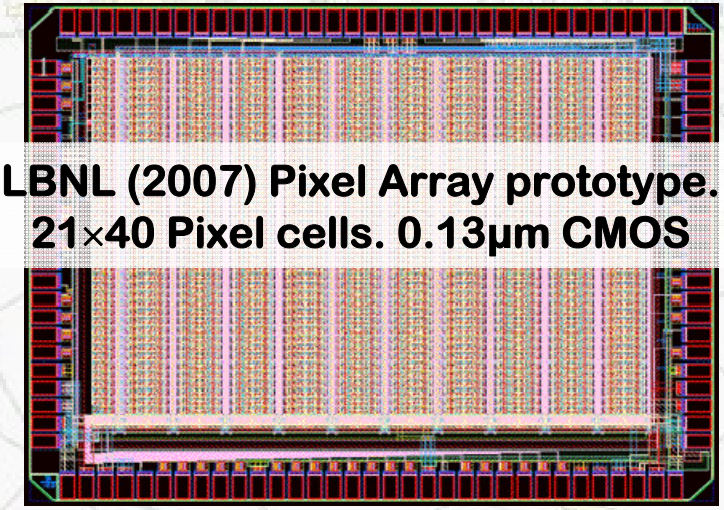
ATLAS Pixel Upgrade Programme

- **Design of a new Front-End chip (FE-I4) for smaller pixel dimensions**
- **B-layer replacement**

→ an intermediate step towards the full upgrade.

Performance improvements for the detector (issues more related to FE chip):

- **Reduce radius → Improve radiation hardness planar , 3D sensors, diamond, gas, …?)**
- **Reduce pixel cell size and architecture related dead time (→ deign FE using 0.13 µm 8 metal CMOS)**
- **Reduce material budget of the b-layer (~3% X_0 → 2.0–2.5% X_0)**
- **increase the module live fraction (→ increase chip size, > 12×14 mm²) .**



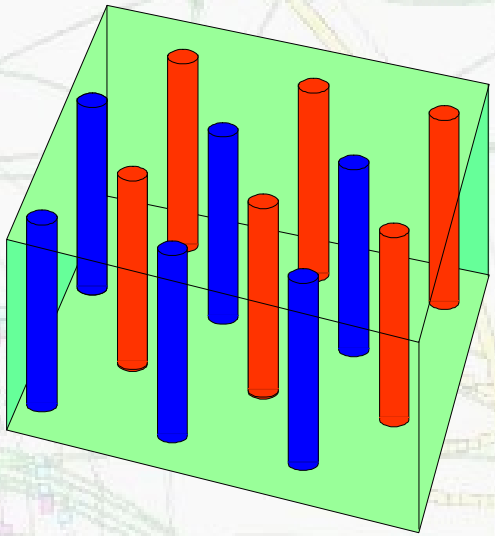
LBNL (2007) Pixel Array prototype. 21×40 Pixel cells. 0.13µm CMOS

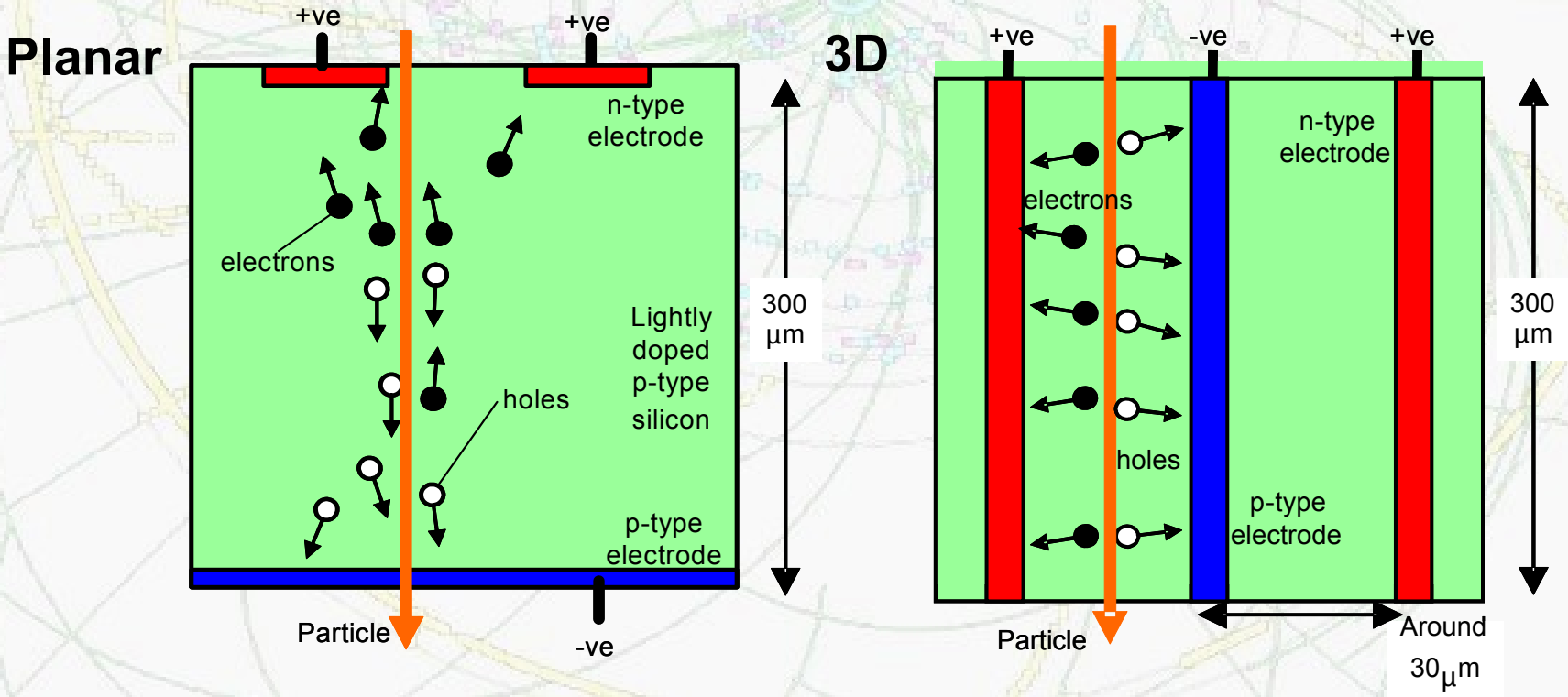
Main Parameter	*Value*	*Unit*
Pixel size	50 x 250	µm²
Input	DC-coupled negative polarity	
Normal pixel input capacitance range	300÷500	fF
In-time threshold with 20ns gate	4000	e
Two-hit time resolution	400	ns
DC leakage current tolerance	100	nA
Single channel ENC sigma (400fF)	300	e
Tuned threshold dispersion	100	e
Analog supply current/pixel @400fF	10	µA
Radiation tolerance	200	MRad
Acquisition mode	Data driven with time stamp	
Time stamp precision	8	bits
Single chip data output rate	160	Mb/s

FE-I4 (B-layer Replacement) Specifications: main parameters

3D Silicon Sensors

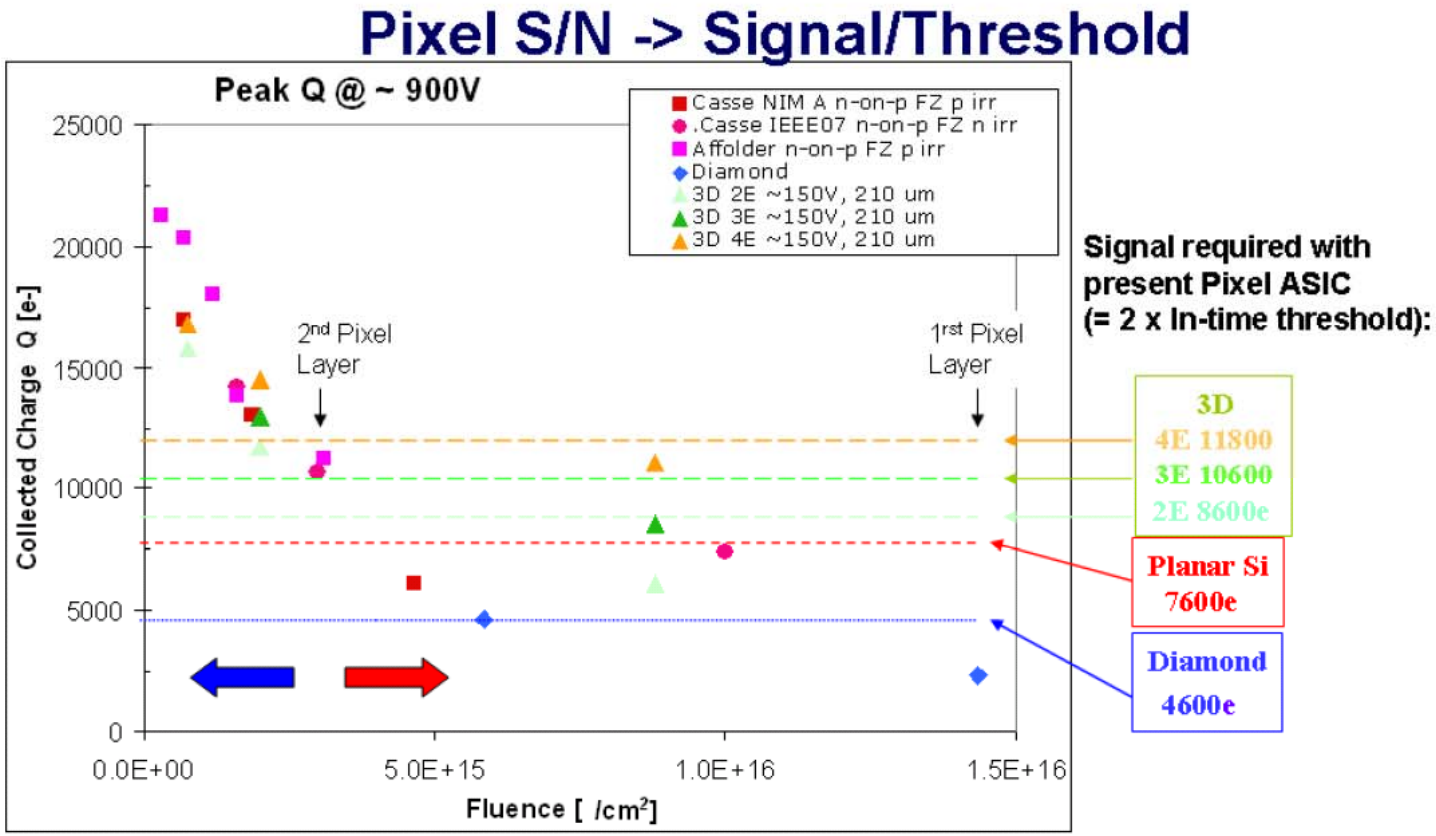
- Array of electrode columns passing through substrate
- Electrode spacing << wafer thickness (e.g. 30μm:300μm)
- Benefits
  - $V_{depletion}$ α (Electrode spacing)^2
  - Collection time α Electrode spacing
  - Reduced charge sharing
- More complicated fabrication – micromachining
- Reduced efficiency in columns
- More columns per pixel increases capacitance





Radiation Hardness Comparison

Signal/2x In-time Threshold (from H. Sadrozinski Jun08 ATLAS talk):



Need to optimize FEE

Marginal performance for innermost Pixel Layer

With current FE threshold limitations, innermost pixels could need frequent replacement

Further possibilities? Gas (*eg* Gossip), others?

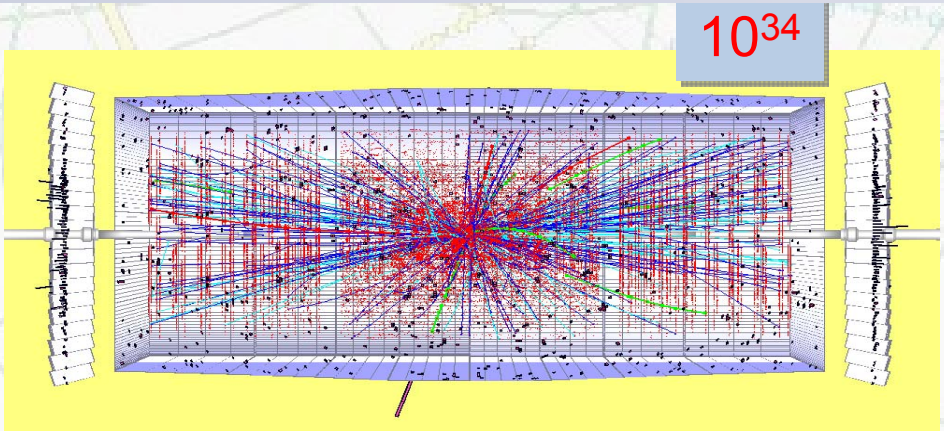
CMS Tracking at the Super-LHC

- **Pixel Upgrade**: 3 layers (4 layer option) 3 disk in each endcap

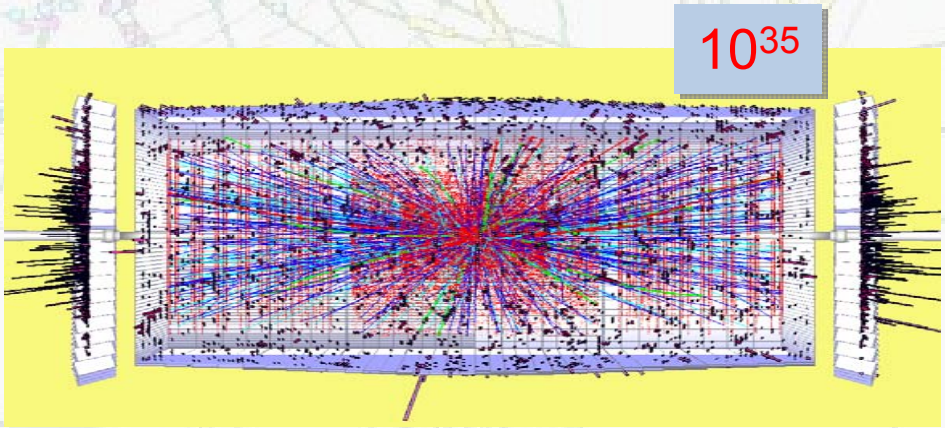
– Detector technology
  - Single sided **n-on-p sensors** (more rad-hard) instead of n-on-n (fallback)
  - Evaluating **3D sensors** industrialization for innermost **layer at 4 cm**.

– Readout Chip
  - Double buffer size (in 250 nm CMOS extra 0.8 mm needed for chip periphery)
  - Further gains possible with 130 nm CMOS but R&D needed

– Layout, mechanical assembly, and cooling (aim at material reduction of about a factor of 3 in barrel and 2 in forward)
  - $C0_2$ cooling (as in VELO for LHCb)
  - Low mass module construction and simplified thermal interfaces
  - Further material reduction to be acheived with on module digitization



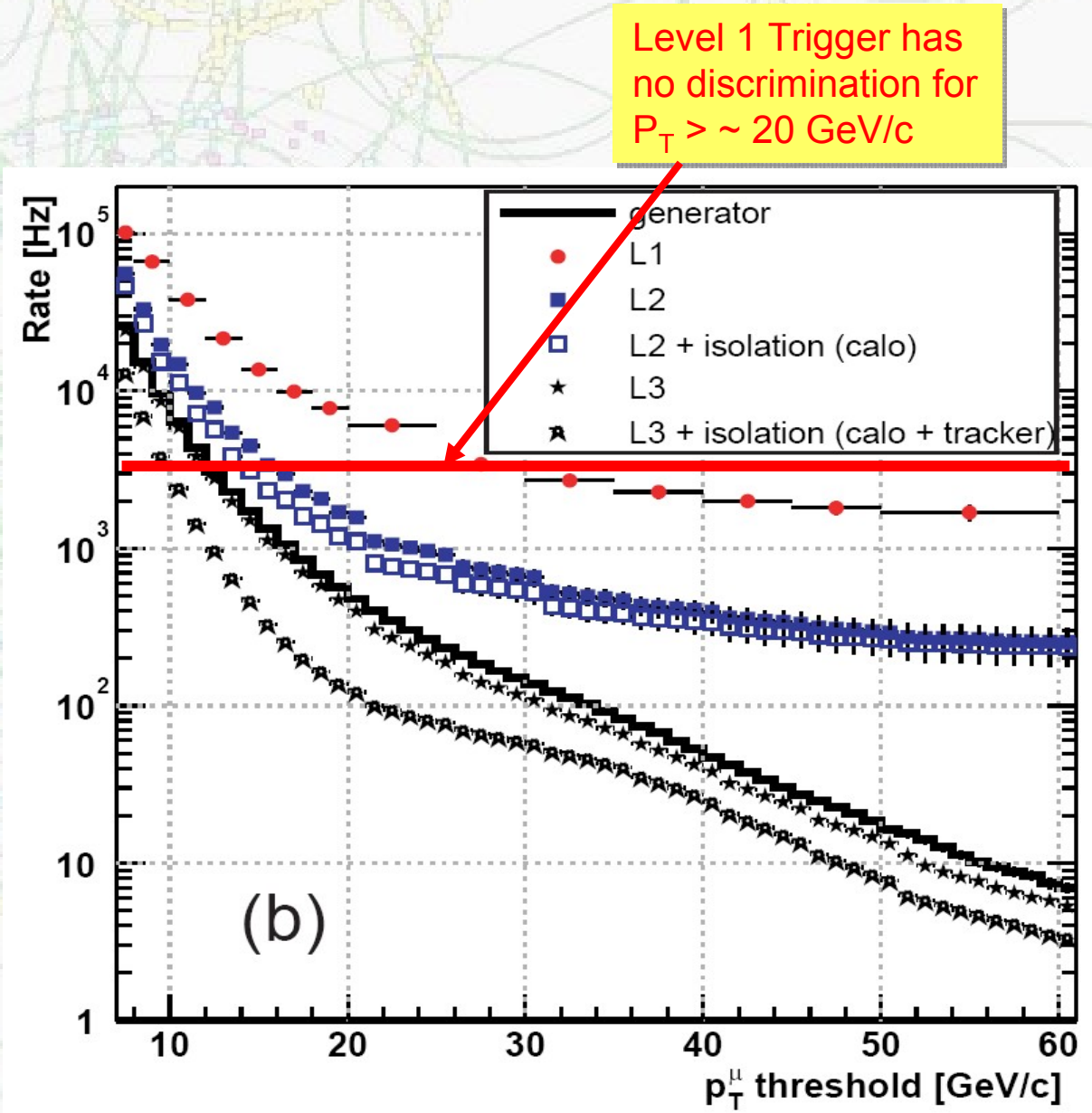
Full LHC luminosity ~20 interactions/bx



SLHC luminosity ~300-400 interactions/bx

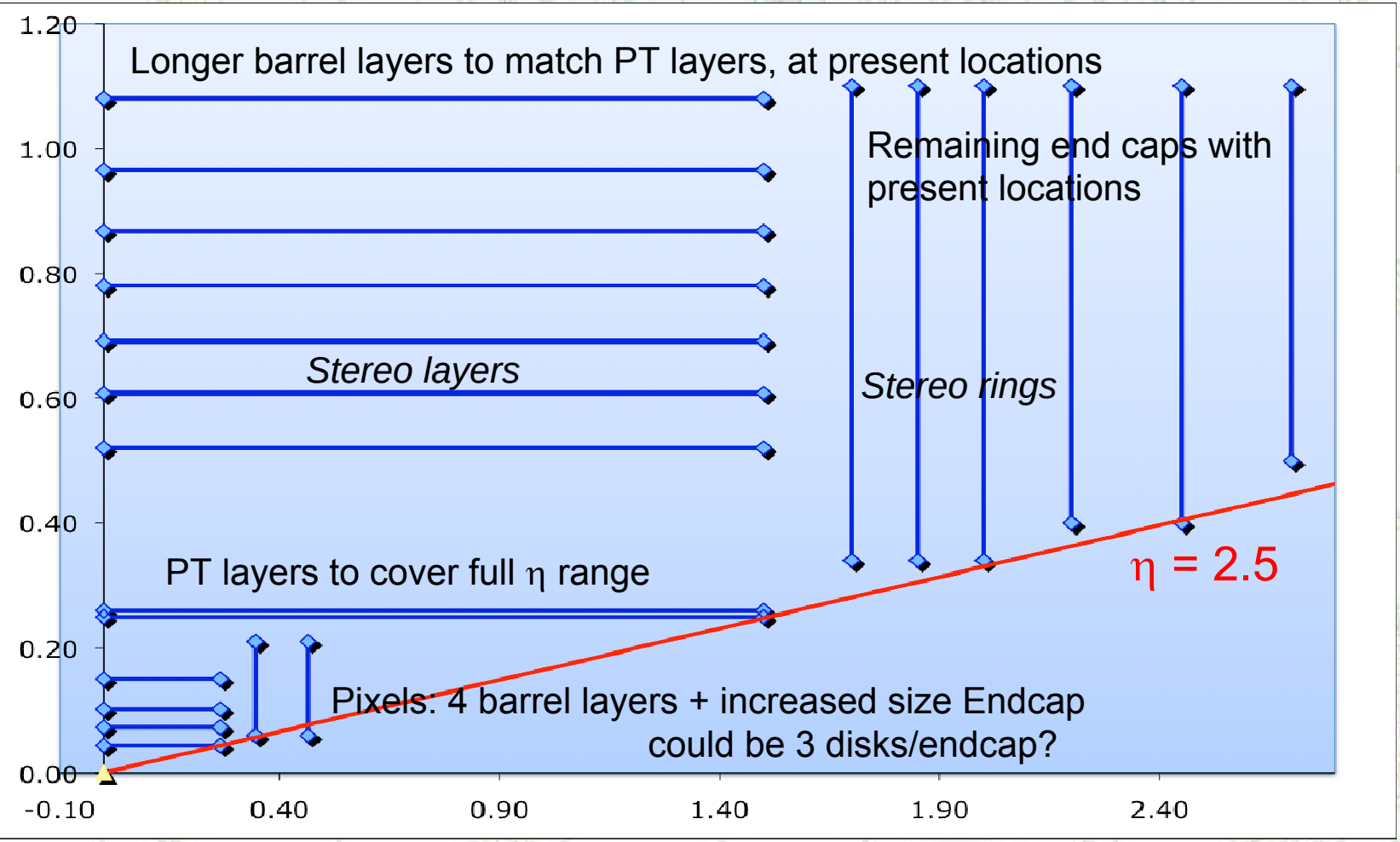
CMS Phase II – Tracking Trigger

- The trigger/DAQ system of CMS will require an upgrade to cope with the higher occupancies and data rates at SLHC
- **One of the key issues for CMS is the requirement to include some element of tracking in the Level 1 Trigger**
  - One example: There may not be enough rejection power using the muon and calorimeter triggers to handle the higher luminosity conditions at SLHC
- Adding tracking information at Level 1 gives the ability to adjust P_T thresholds
- Single electron trigger rate also suffers
  - *Isolation criteria are insufficient to reduce rate at* $\mathrm{L} = 10^{35}\,cm^{-2}.s^{-1}$



CMS Triggering

MS can't keep trigger rate at 100 kHz at SLHC without P_T information from tracker
major new feature for CMS tracker - ideas how to do it are still developing
urrent assumption is that there will probably be dedicated PT layers, providing prompt trigger informatio
i.e. different from more conventional, triggered pipeline chip, layers
everal ideas for triggering layers summarised here



one possible "strawman" layout

X section through one quarter of tracker

Triggering Possible Approaches

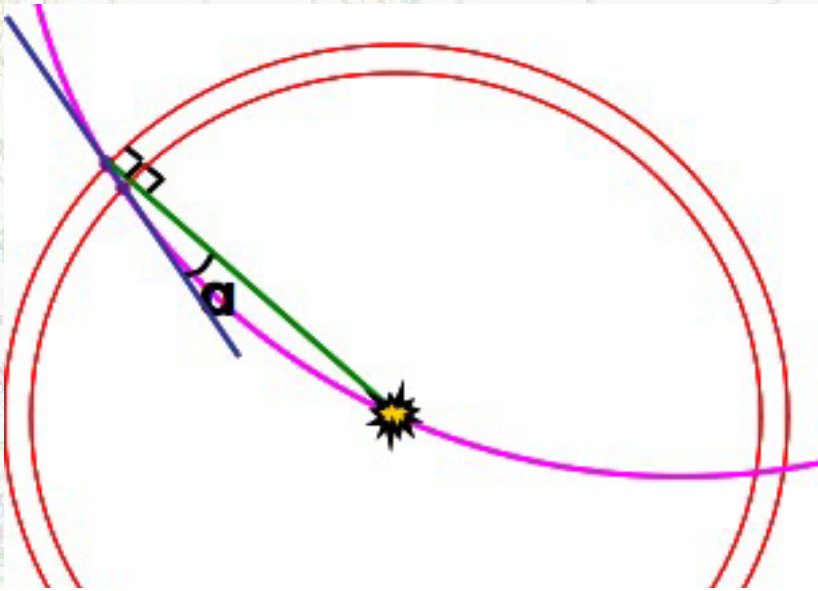
Stacked tracking

correlate hits from tracks in closely spaced layers
high PT track passes through pixels directly above each other
needs separate chip to perform correlation

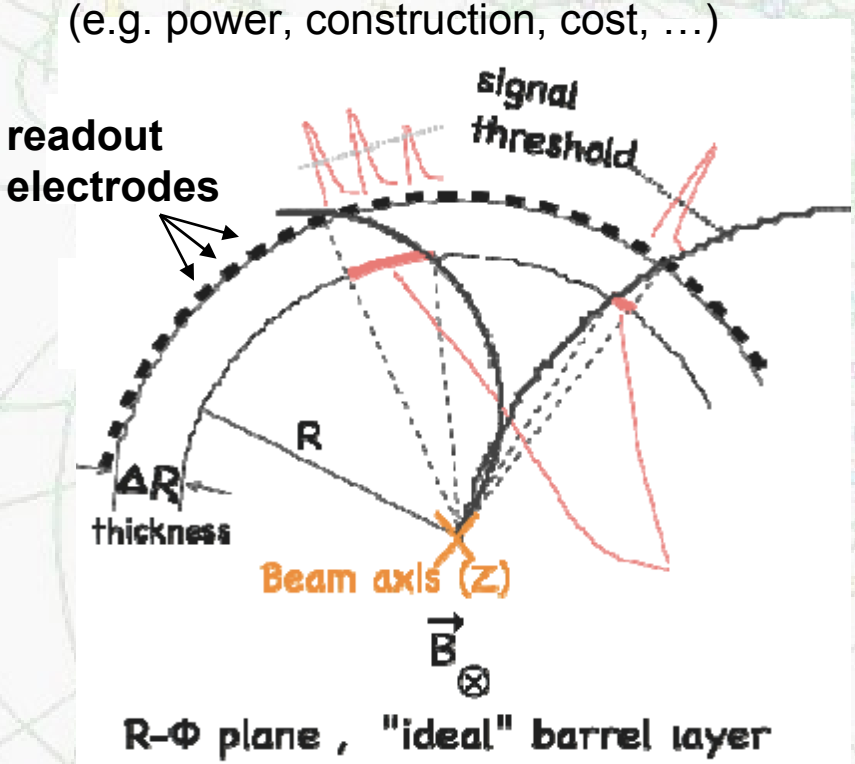
Cluster width discrimination

high PT track -> narrow cluster width

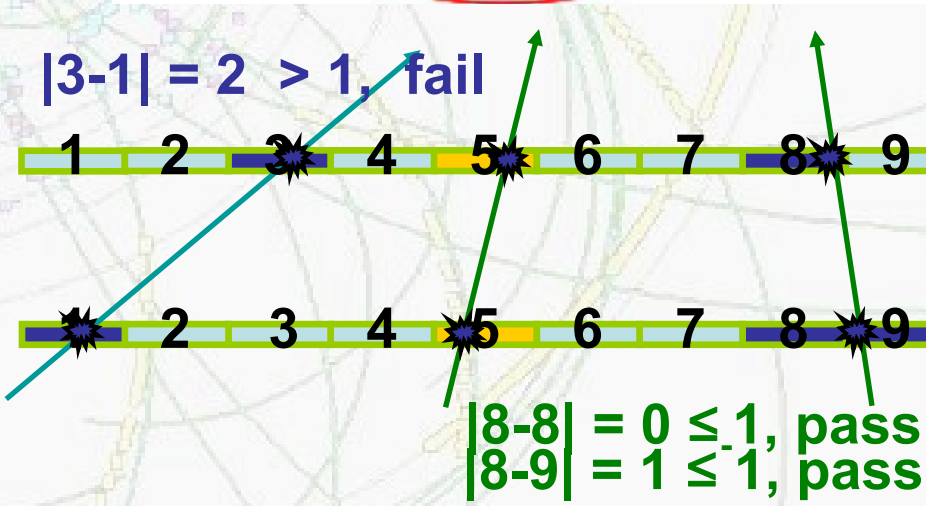
basic concepts clear but need to understand issues associated with practical implementations
(e.g. power, construction, cost, …)



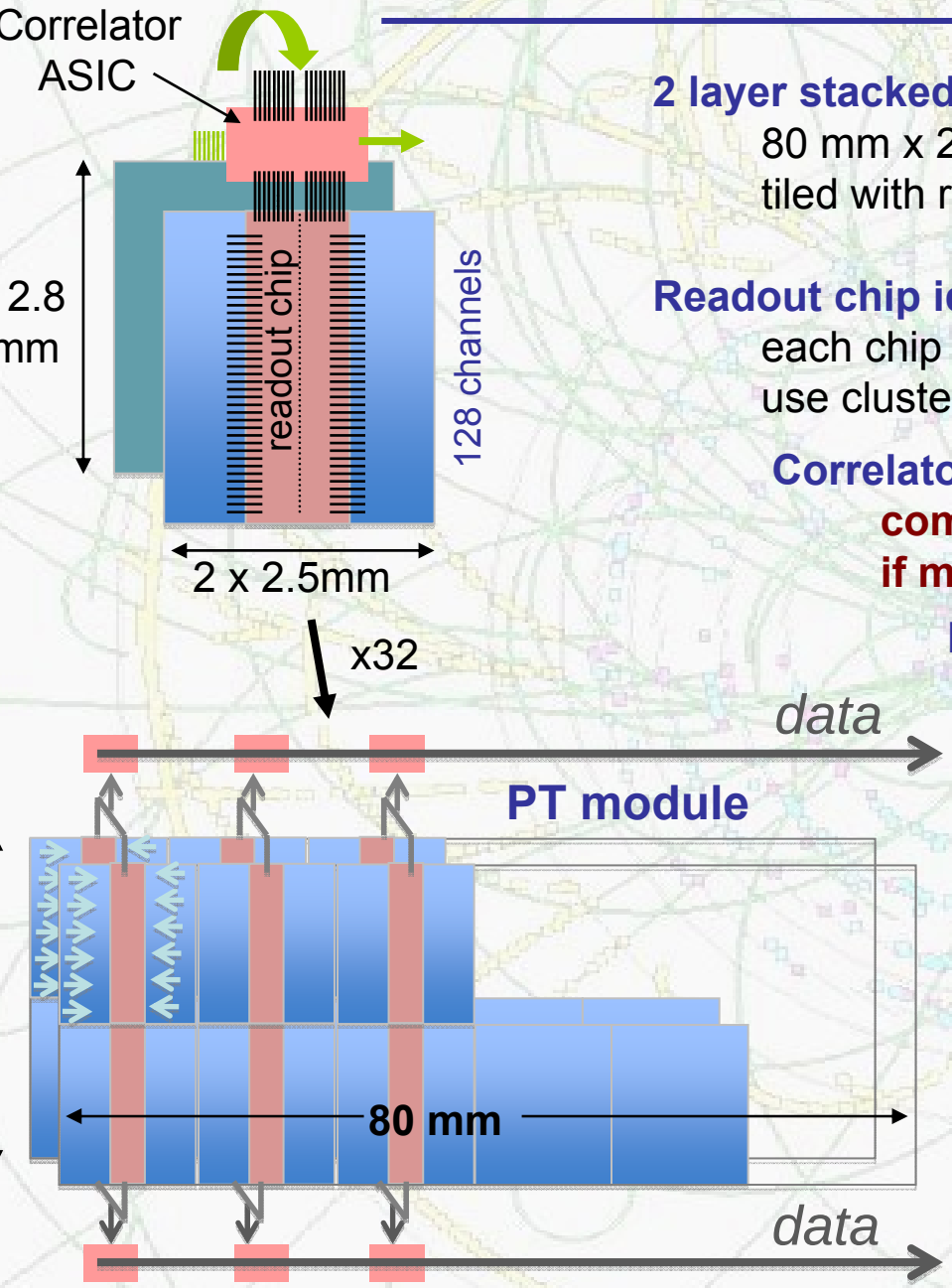
Stacked Tracking for CMS at Super-LHC, *J.Jones et al,* 12th LHC Workshop, 2006



Track momentum discrimination using cluster width in Si strip sensors, *G.Barbagli, F.Palla, G. Parrini,* TWEPP07



Possible P_T Module for Inner Layer



2 layer stacked tracking approach

80 mm x 25.6 mm sensors segmented into 2.5 mm x 100 μm pixels tiled with readout chips – could be wire bonded for easy prototyping

Readout chip ideas

each chip deals with 2 x 128 channel columns
use cluster width discrimination to reduce data volume

Correlator

compares hit pattern and address from both layers
if match then shift result off-detector

Data volumes

need to transmit all correlated hit patterns every BX
predicted occupancy + reduction from correlation
=> 1 link can serve 2 PT modules

Link power

need ~ 3000 PT modules for 3m length cylinder, r=25c
so 1500 links (@2.56 Gbps) => **3 kW** @ 2W / link

Readout power

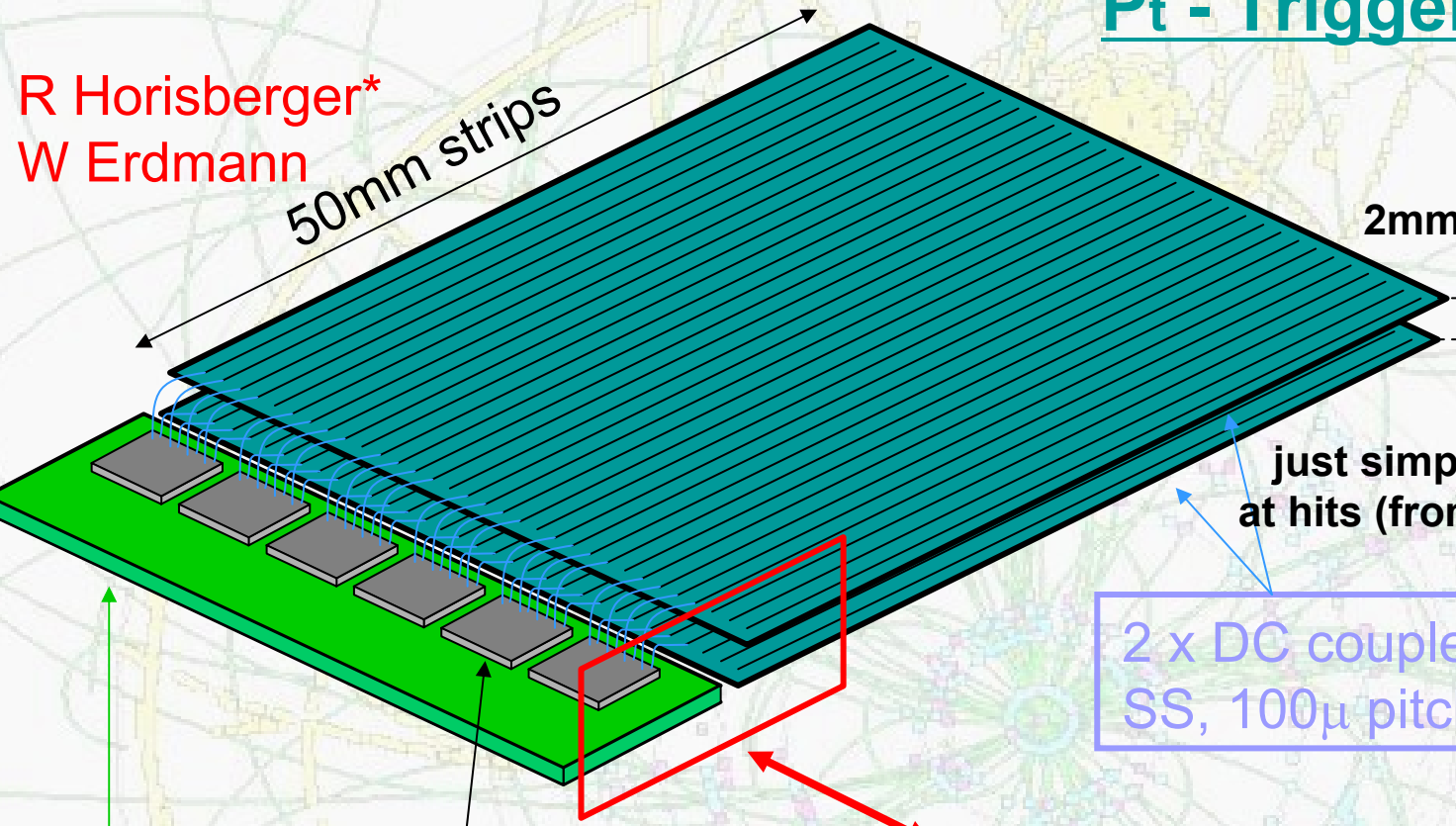
50 μW / pixel (extrapolate from current pixels)
=> **2.4 kW** for 8192 x 2 x 3000 channels

=> this will not be a low power layer

http://indico.cern.ch/getFile.py/access?contribId=15&sessionId=2&resId=1&materialId=slides&confId=36581

Pt - Trigger for TOB Layers

R Horisberger*
W Erdmann

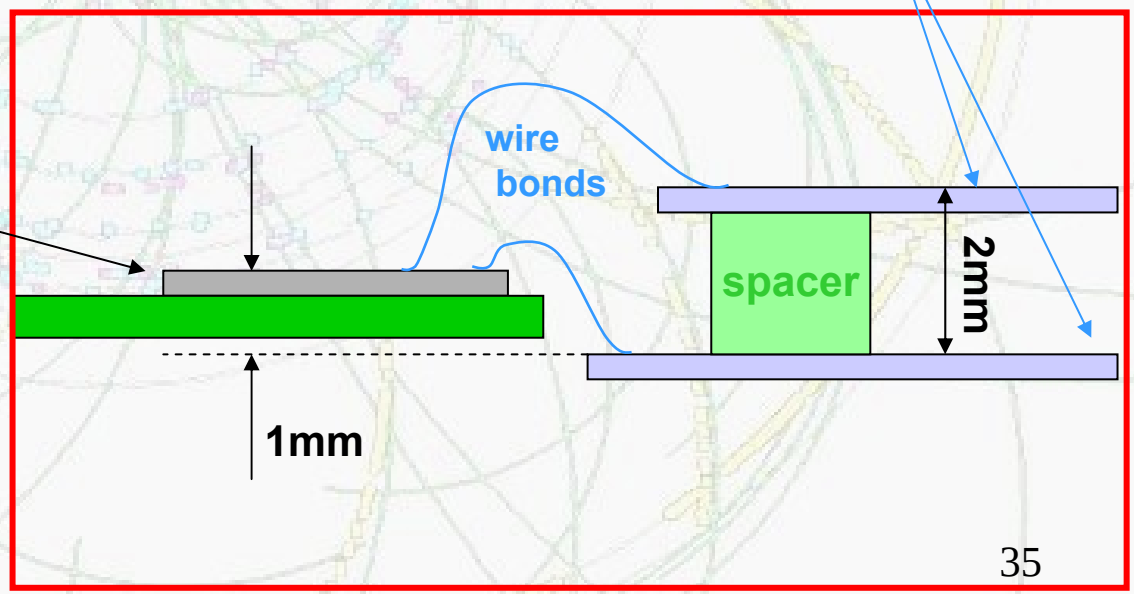


Two-In-One Design
bond stacked upper and lowe
sensor channels to **adjacen**
channels on same ASI
no interlayer communicatio
no extra correlation chi
just simple logic on readout chip, lookin
at hits (from 2 layers) on adjacent channel

2 x DC coupled Strip detectors
SS, 100μ pitch ~8CHF/cm²

Strip Read Out Chip
2 x 100μ pitch with
on-chip correlator

Hybrid



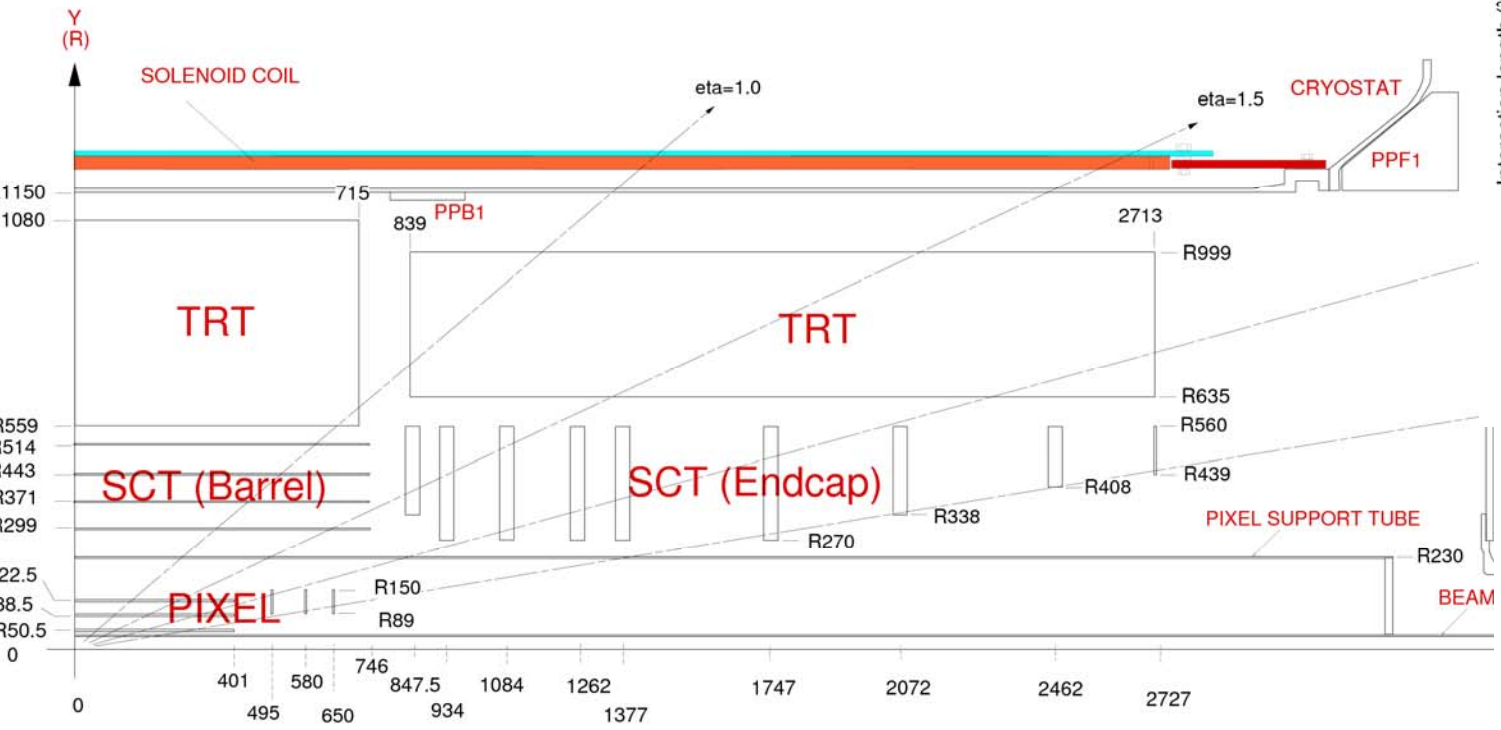
track angular resolution ~20mrad

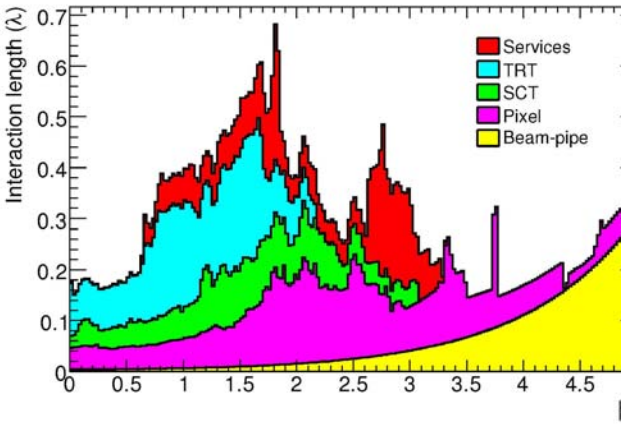
→ good P_t resolution

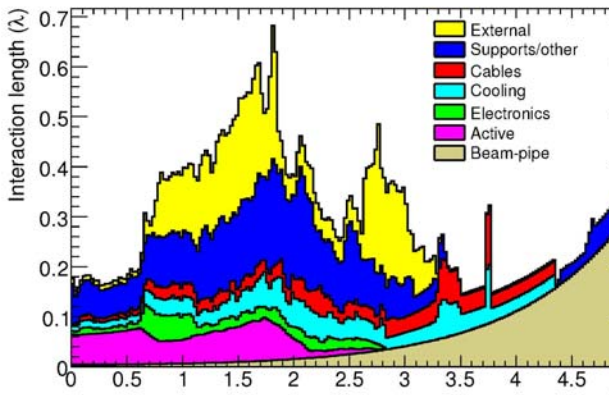
W.E. / R.H.

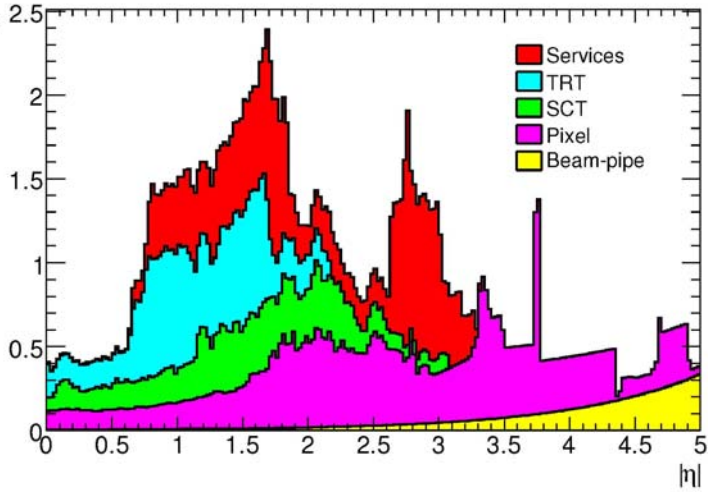
* *http://indico.cern.ch/getFile.py/access?contribId=3&sessionId=0&resId=0&materialId=0&confId=36580*

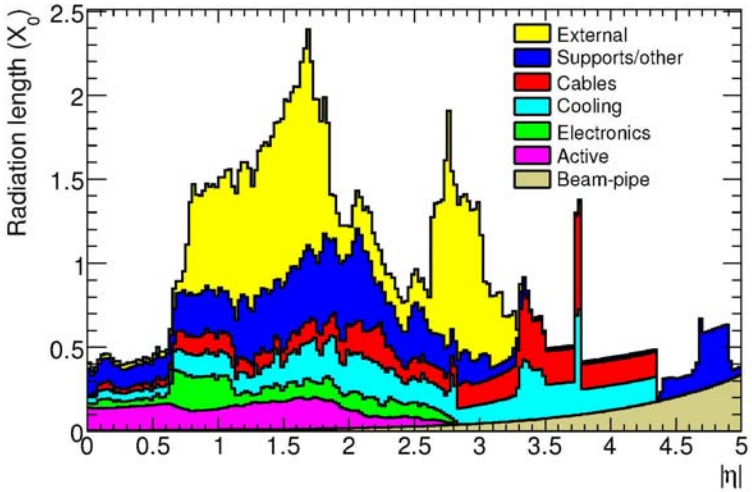
Material in Existing Trackers: ATLAS

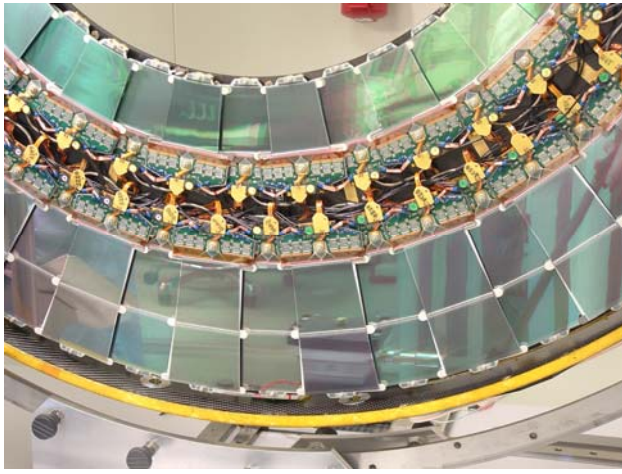






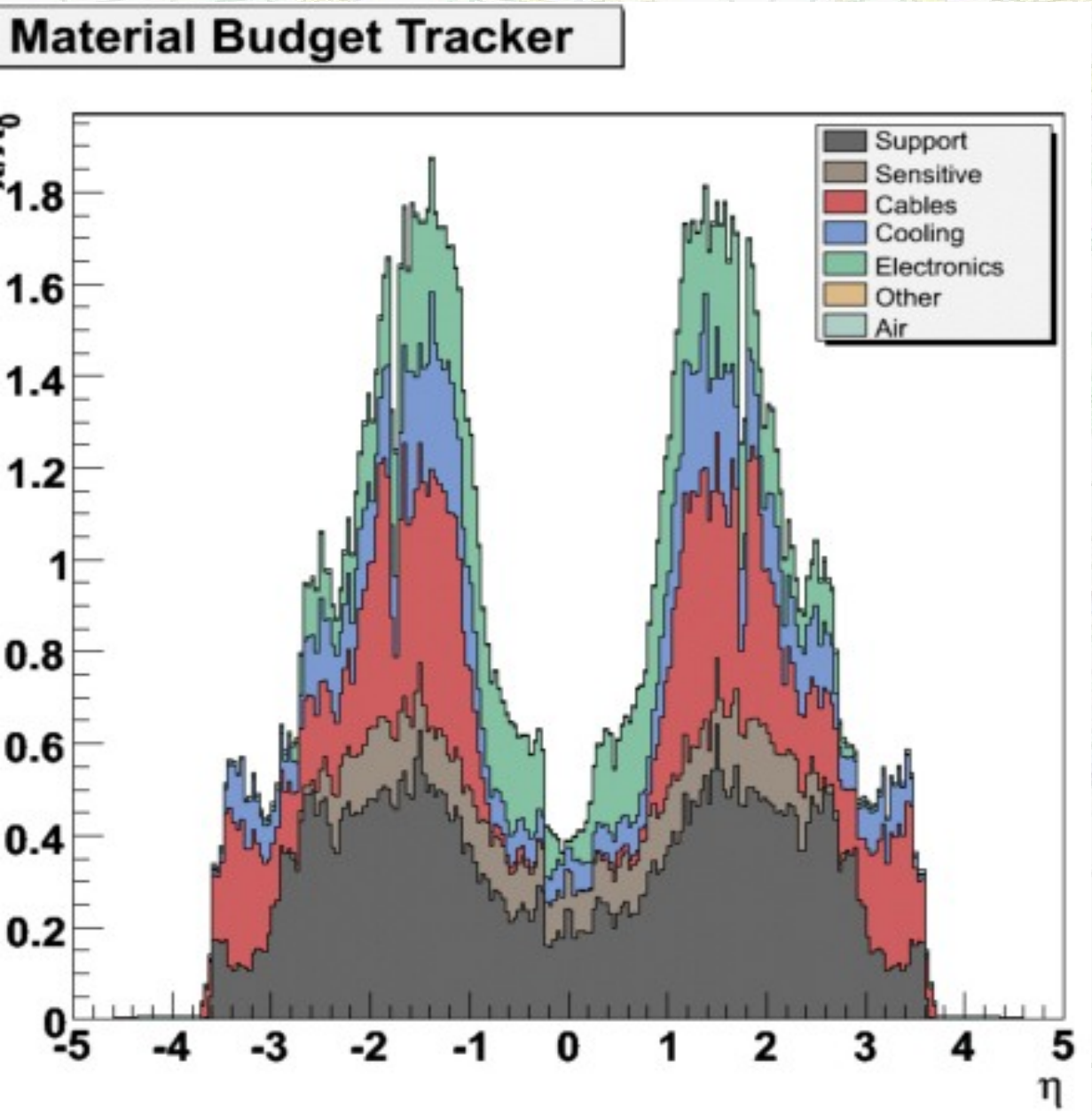




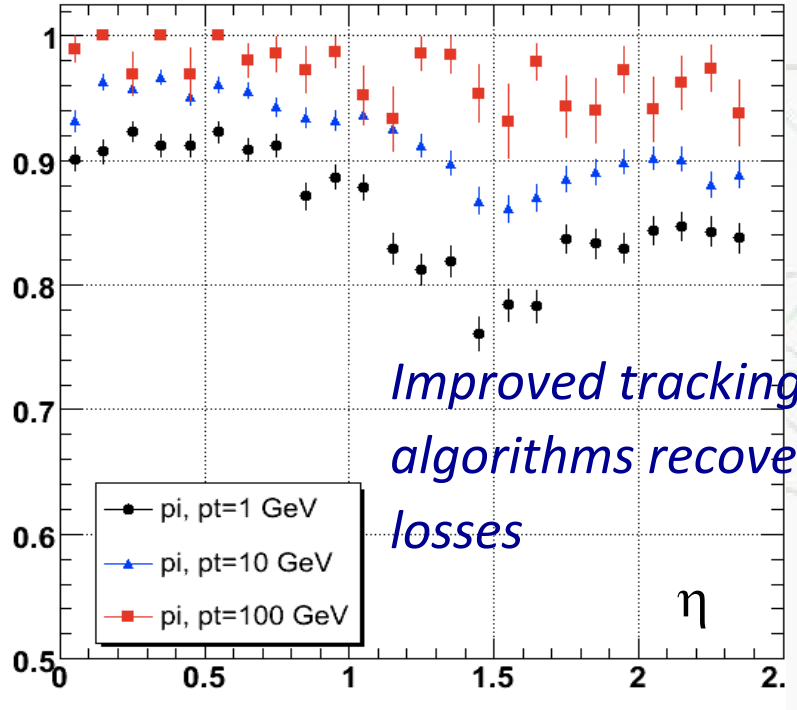


https://twiki.cern.ch/twiki/bin/view/Atlas/AtlasTechnicalPaper

Material in Existing Trackers: CMS



Pion track finding efficiency vs



Improved tracking algorithms recover losses

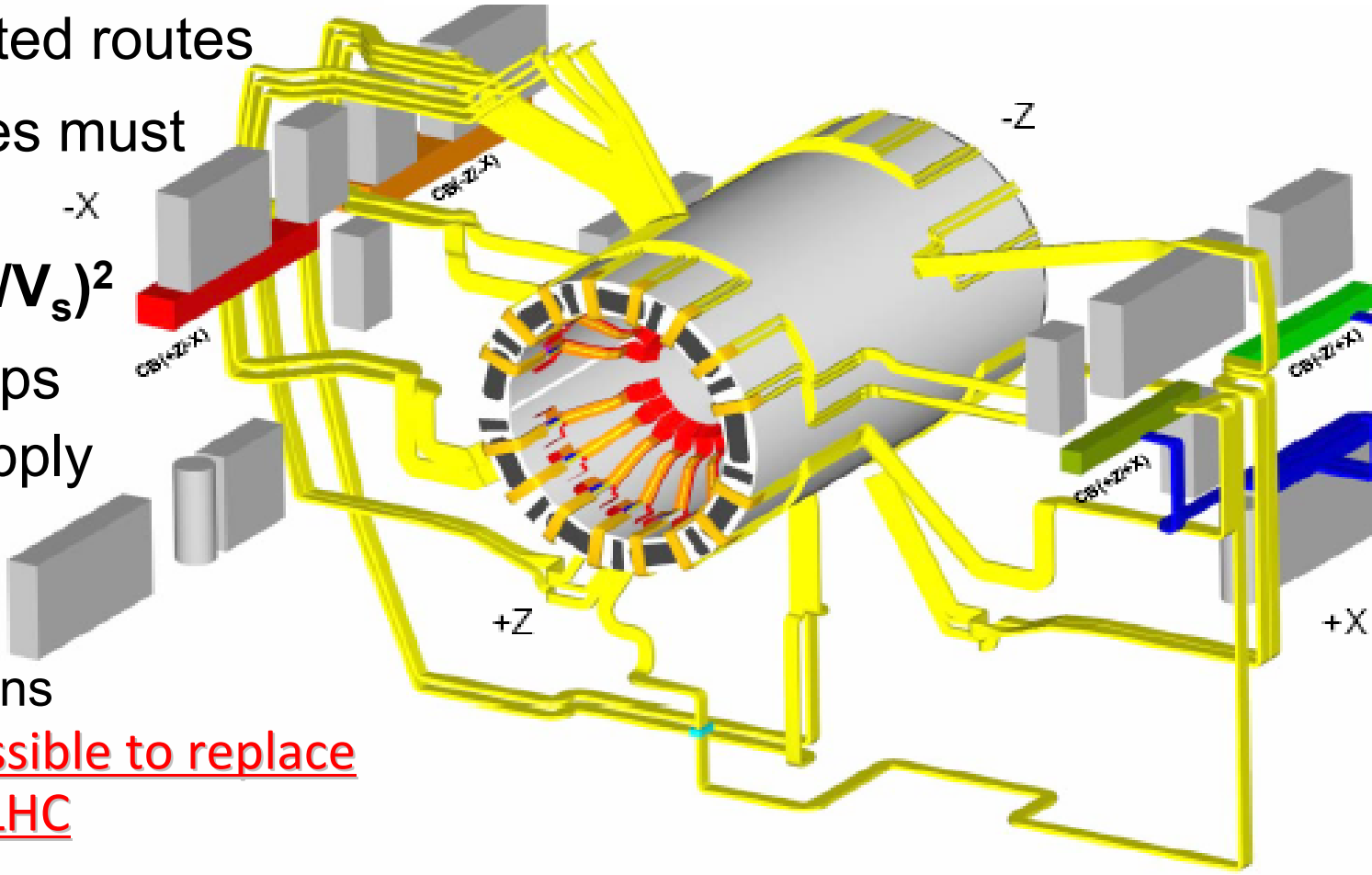
- Reducing power would be beneficia
  can routing improve?
- Present power requirements
  inner microstrips: 400 W.m^{-2}
  pixels: ~2700 W.m^{-2} (pre-rad)

CMS Tracker Services

Major constraint on upgraded system

- Complex, congested routes
- Heat load of cables must be removed
- $P_{cable} = R_{cable}(P_{FE}/V_s)^2$
- Cable voltage drops exceed ASIC supply voltages
  - limited tolerance to voltage excursions

Installation of services was one of the most difficult jobs to complete CMS



It will probably be impossible to replace cables and cooling for SLHC

$P_{FE} \approx 33kW$ $I=15,500A$ $P_S = 300kVA$

Powering Schemes to Reduce Number of Cables

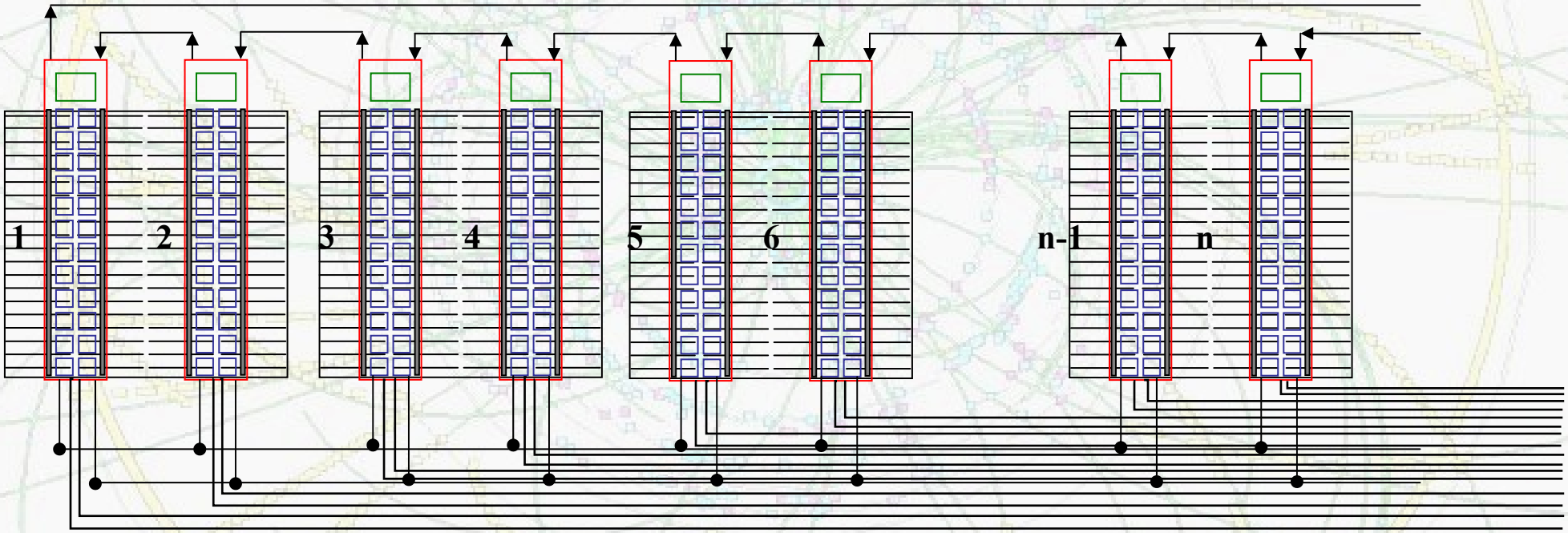
$V_{ABC\text{-}N}$ = 2.5 V; I_{Hybrid} = 2.4 A; 20 hybrids. **Low V + High I ➔ I^2R losses in cables**

(Want power transmission at High V + Low I)

Serial Powering: n=20; $I_H = I_{PS} = 2.4$ A; $V_{PS} = nV_{ABC\text{-}N} = 50$ V

Also saves factor ~8 in power cables/length over SCT

Need detailed studies of failure modes and recovery



DC-DC Conversion : n=20; g =20; $I_{PS} = n/g\ I_H = 2.4$A; $V_{PS} = gV_{ABC\text{-}N} = 50$V

Parallel powering also saves factor ~8 in power cables as for Serial Powering

Issues with switched capacitors (noise?) and need for custom design to get large g

(Independent powering with DC-DC costs too many cables)

ATLAS Serial Powering Results

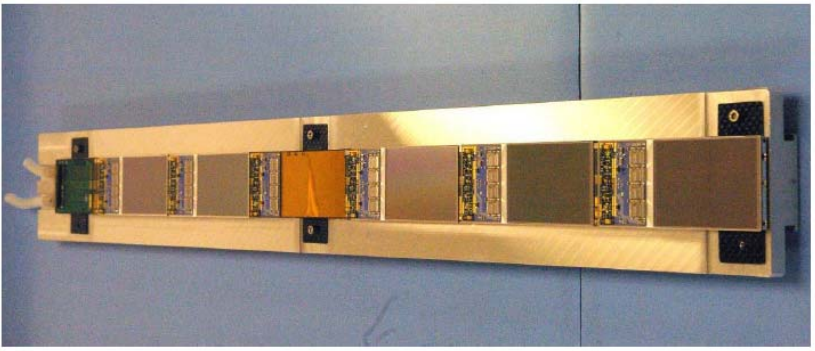


Figure 39. Six module (5 sensors; 6 hybrids) stave with serial powering built in the UK. Another version stave was build at LBNL.

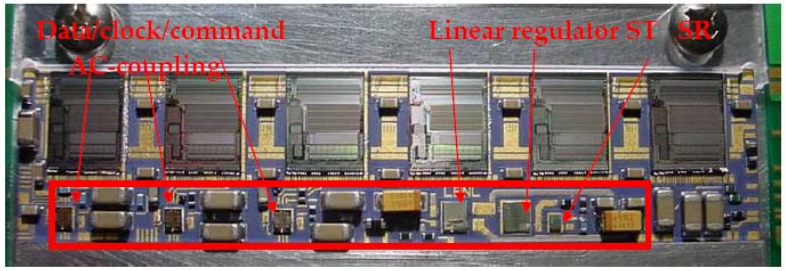
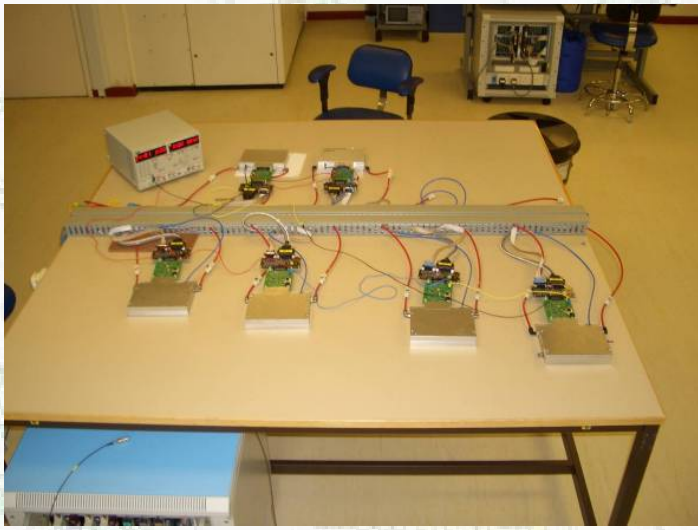


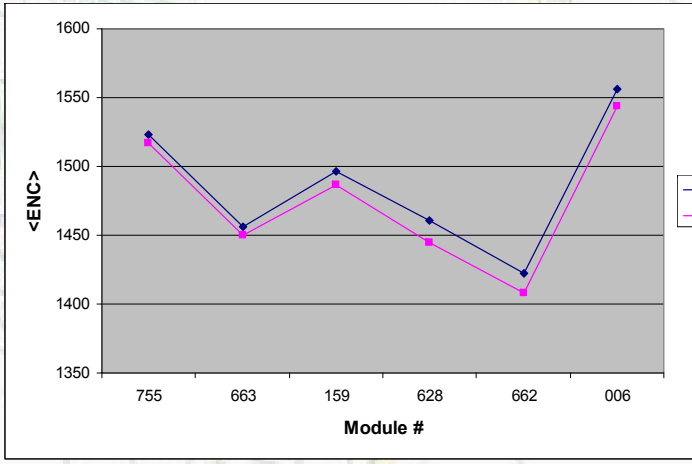
Figure 40. Ceramic hybrid (LBNL) with six ABCD Chips and Serial Powering Circuitry.

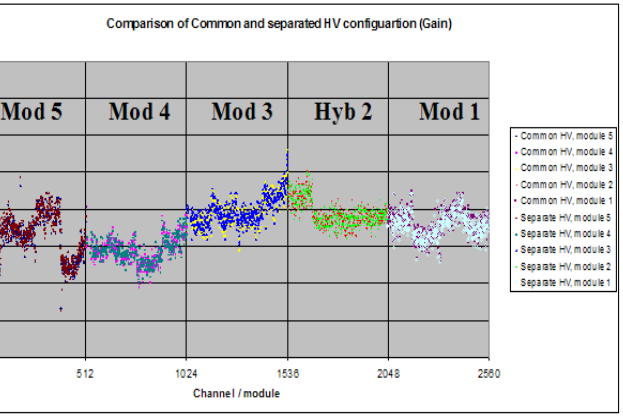
All studies using serial powering and multi-drop LVDS now give results consistent with individual hybrid/module powering



Upgrade PO

6 SCT module noise studies





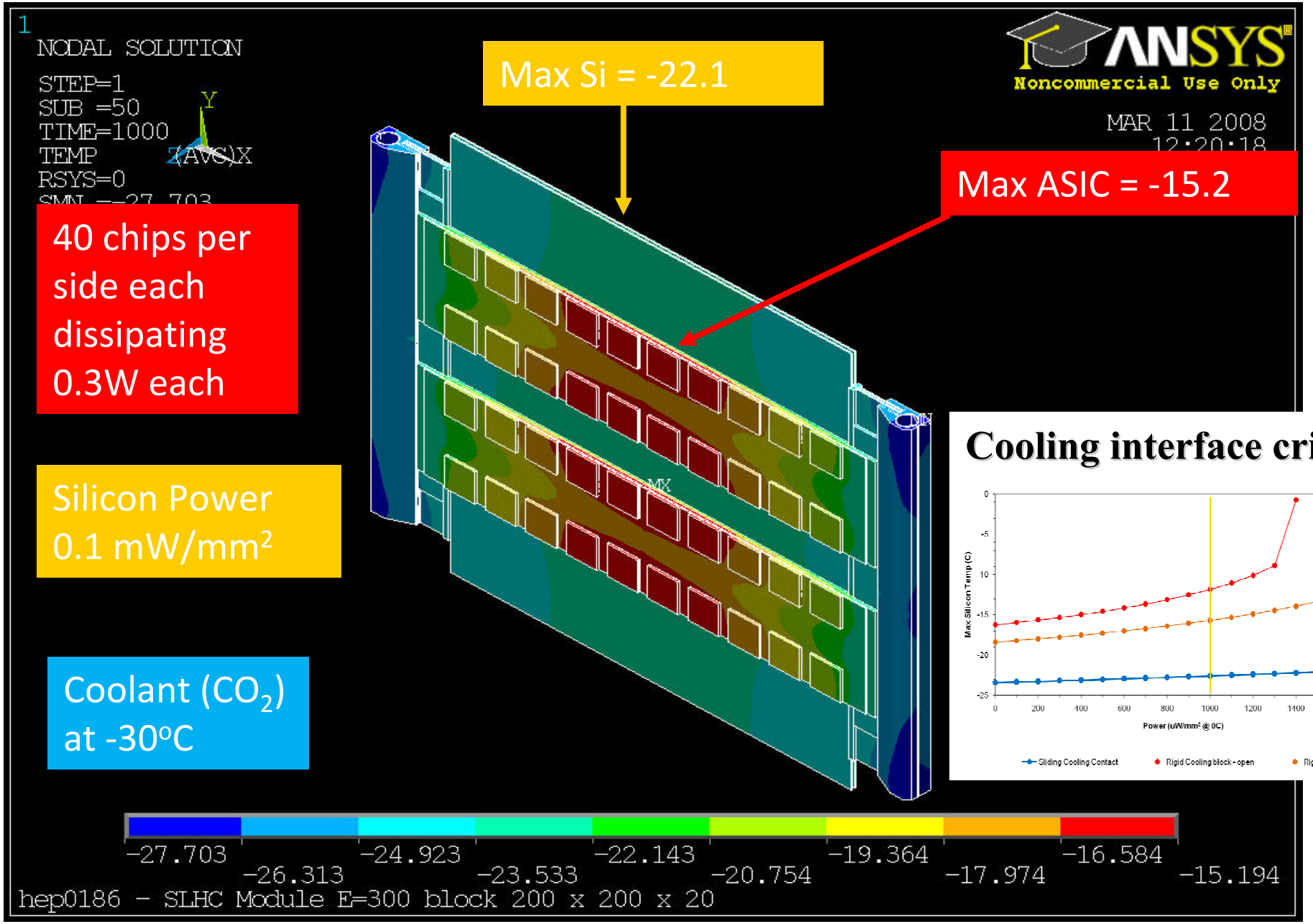
4 V x 30 hybrids = 120 V (0.8 A)

30 Hybrid LBL Test Stave

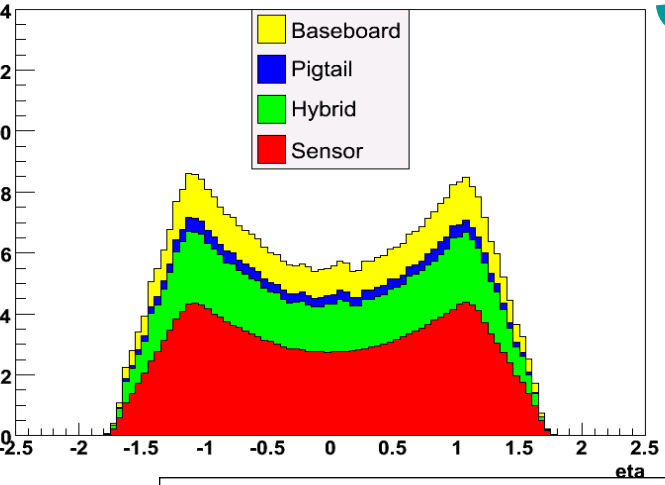
Module Stave Comparison of ommon and separated HV

Material Needed to get Heat to Cooling

(FEA with coolant to tube wall heat transfer and silicon self-heating effects)



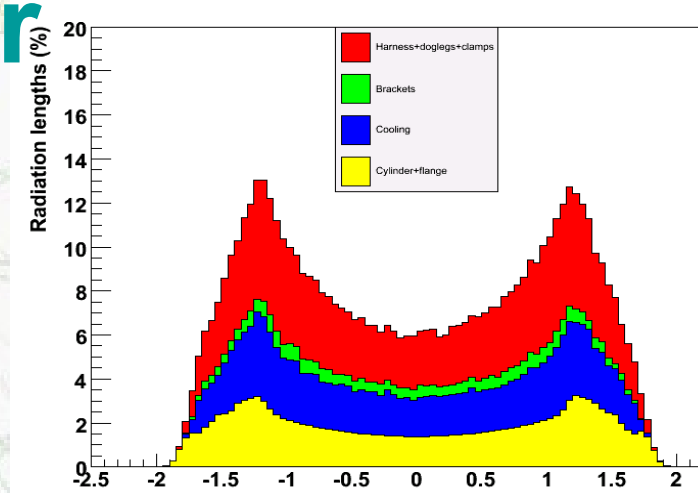
Impact of Hybrid Material on Current Silicon Tracker



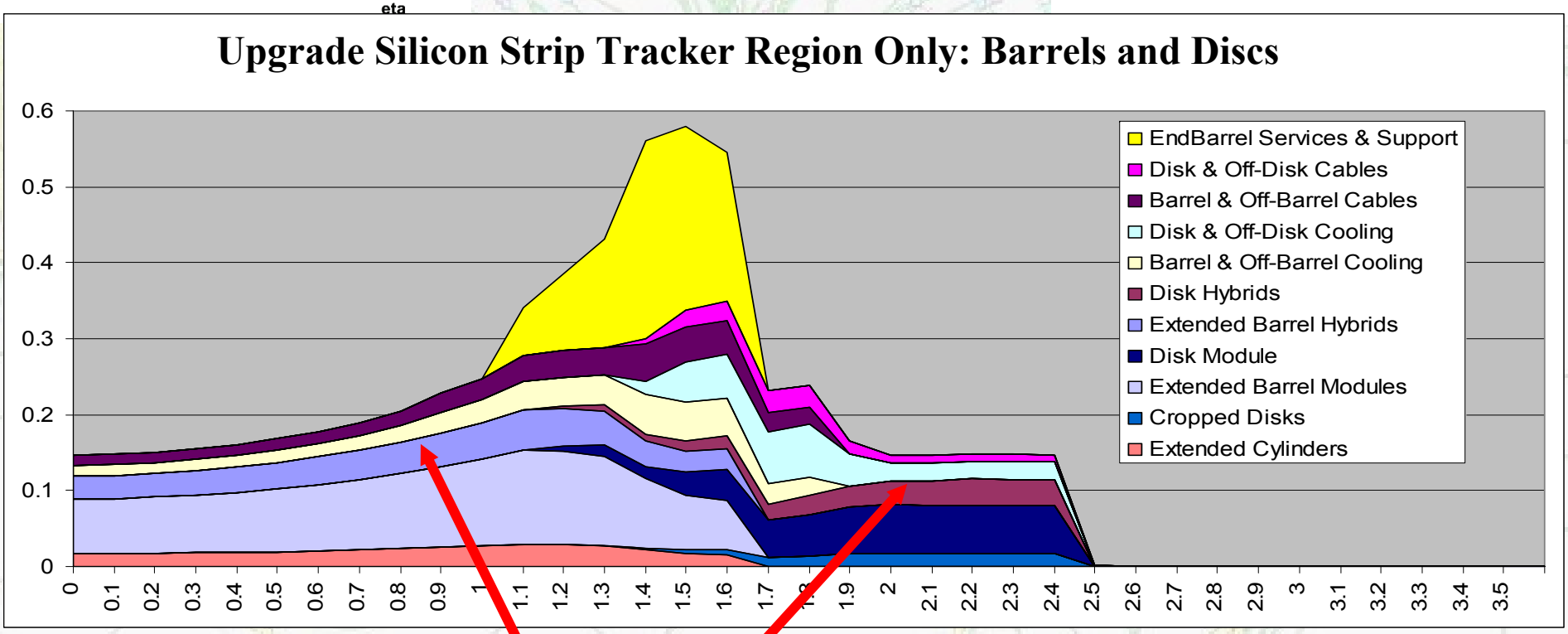
Current Silicon Tracker
(4 barrel strip layers)

Module Material

Support Material



Upgrade Silicon Strip Tracker Region Only: Barrels and Discs

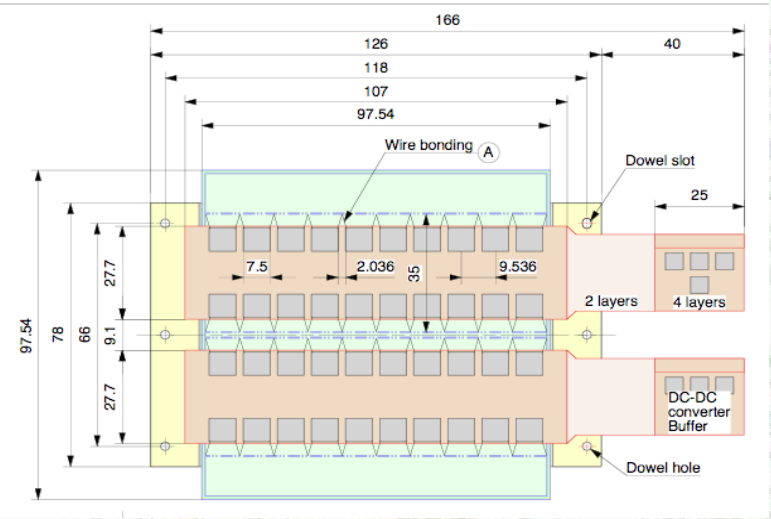


Hybrids

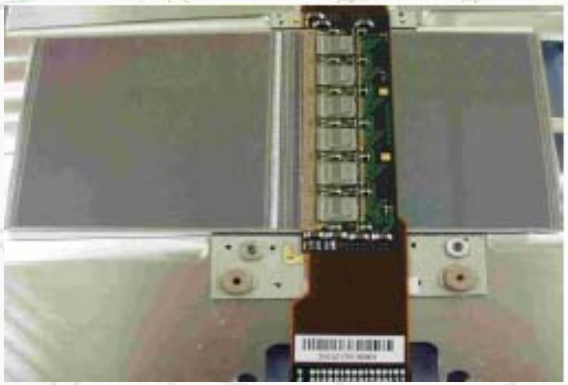
Hybrids area per module ×2 at SLHC becoming half of overall module materi

Double-sided Module Material Estimates

lew ATLAS SLHC-Tracker Module
subject to design - indicative numbers)
0 ASIC's, thickness matters
300µm assumed)



Old ATLAS Barrel Module
2 ASIC's of 300µm thickness



Module Short Strip (Low Radius)	Rad len (%)	Mass (gm)
Silicon sensors w/thermal adhesive	0.69	14.35
Baseboard w/AlN facings	0.30	10.40
ASIC's w/conductive adhesive and w-bonds	0.19	4.08
Hybrid w/passive compo's	0.77	25.26
Hybrid-facing thermal adhesive	0.00	0.11
Total	1.95	54

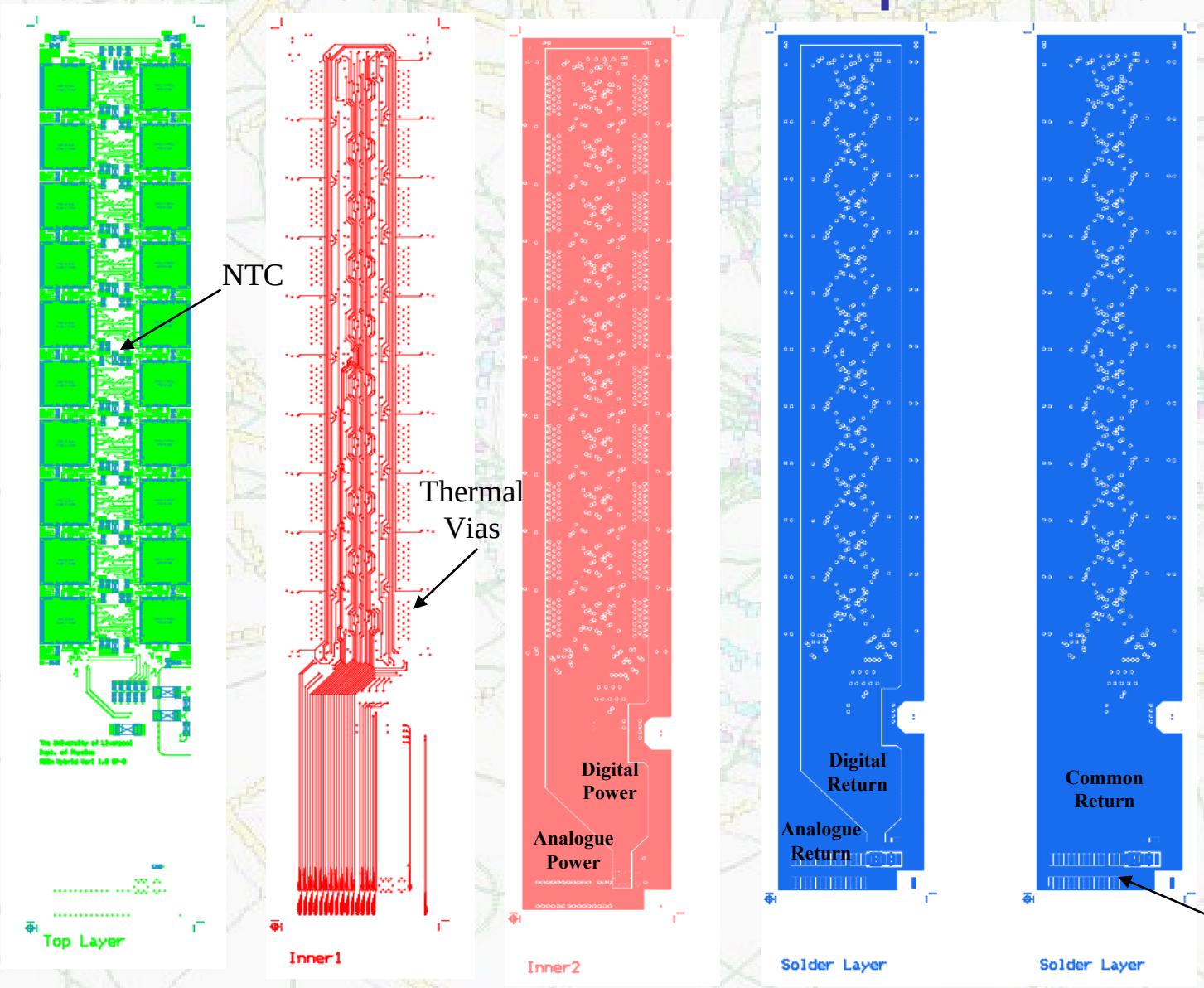
Module Long Strip (High Radius)	Rad len (%)	Mass (gm)
Silicon sensors w/thermal adhesive	0.69	14.35
Baseboard w/AlN facings	0.20	6.71
ASIC's w/conductive adhesive and w-bonds	0.05	1.02
Hybrid w/passive compo's	0.31	10.10
Hybrid-facing thermal adhesive	0.00	0.05
Total	1.24	32

Table 1
Radiation lengths and weights estimated for the SCT barrel module

Component	Radiation length [%Xo]	Weight [gr]	Fraction [%]
Silicon sensors and adhesives	0.612	10.9	44
Baseboard and BeO facings	0.194	6.7	27
ASIC's and adhesives	0.063	1.0	4
Cu/Polyimide/CC hybrid	0.221	4.7	19
Surface mount components	0.076	1.6	6
Total	1.17	24.9	100

SLHC Hybrid Realisation

(Already done away with fan-ins by adopting direct bonding and reduced traces to minimum compatible with ASIC dimensions)



Top Layer | Inner1 Layer | Power Layer | Split Ground | Single Ground

Hybrid construction is of 50µm dielectrics (Kapton) using 18µm Cu.
Typically 100µm track & gap
With 375µm via lands.

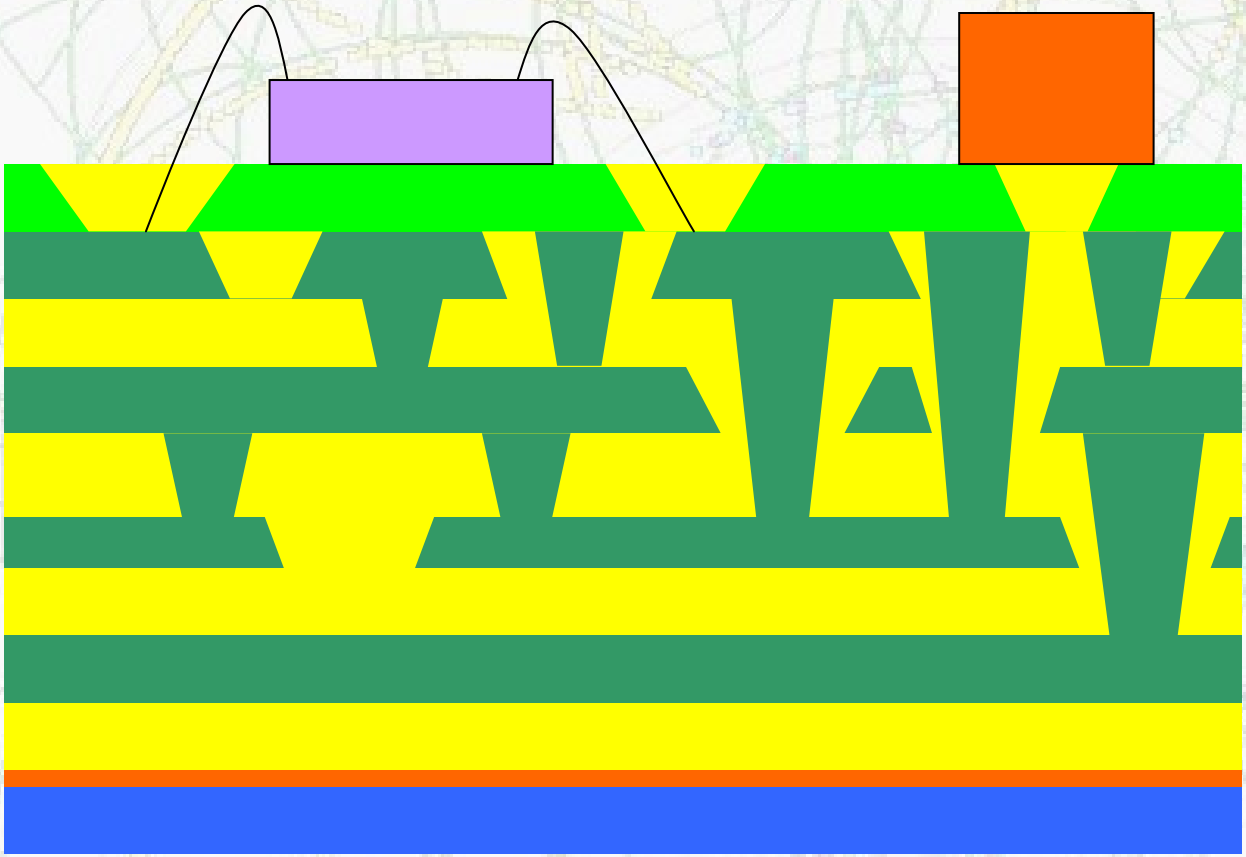
Layer Stack order (top – down):

1)Top Layer
2)Inner1 Layer
3)Power
4)Ground

Hybrid Dimensions: 24mm x 147mm

Split or Single Ground plane for both Analogue and Digital Power supplies

Direct Processing of Hybrid Circuit on Silicon Sensor (3D Integration Technology)



SMD Solder (FC4b)

Wirebond + fanin Au (FC4a)

3rd dielectric BCB (FD3) / via fill (FV3)

Gnd/trace2 Cu (FC3)

2nd dielectric BCB (FD2) / via fill (FV2)

Power/trace1 Cu (FC2)

1st dielectric BCB (FD1) / via fill (FV1)

Shield layer Cu (FC1)

BCB (Benzocyclobutene) 5–15μm

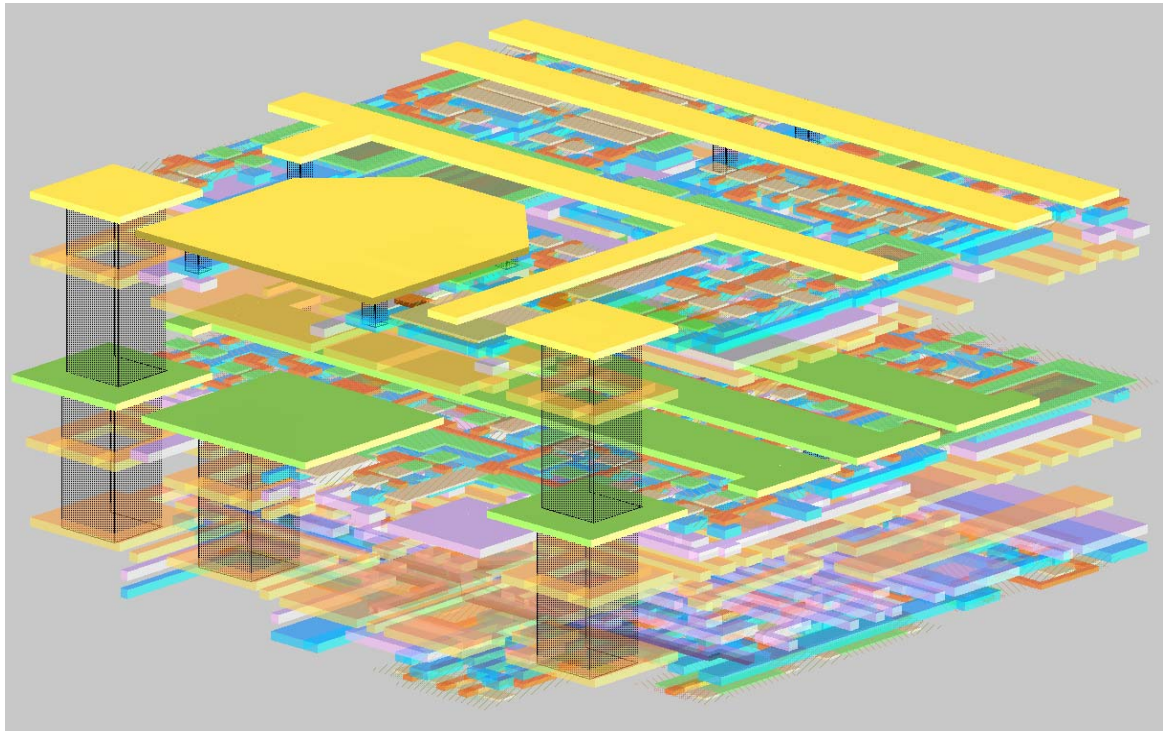
Si base

Does away with need for hybrid substrate and thick-film processing.
Prototyping for ATLAS underway with Acreo (Sweden)

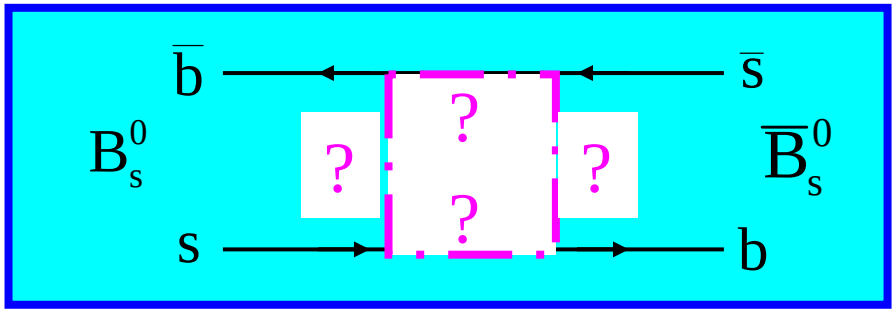
Ultimate Interconnection: Vertical Integration

deal solution for reducing material and easing assembly in pixel detector system and attractive for aspects of rest of tracker array f affordable

- This has been a “dream” for many years
- More complex detectors, low mass
- Liberate us from bump/wire bonding



LHCb Flavour Physics at High Luminosity



Complementary to ATLAS / CMS direct searches

New particles are discovered

– LHCb measure flavour couplings through loop diagrams, understand nature of new physics

No new particles are found

– LHCb probe NP at multi-TeV energy scale,

– Like in the past (e.g. top mass prediction) loop processes allow discoveries beyond direct production limits

Requires high precision = high luminosity

Physics Programme

Limited by Detector

But **NOT** Limited by LHC

Upgrade to extend Physics reach

- Read out full detector at 40MHZ
- Displaced vertex triggering at first level in CPU farm

Timescale, 2013-2014

- First LHC upgrade period

Modest cost compared with existing accelerator infrastructure

Independent of LHC upgrade
•SLHC not needed
•But compatible with SLHC phase

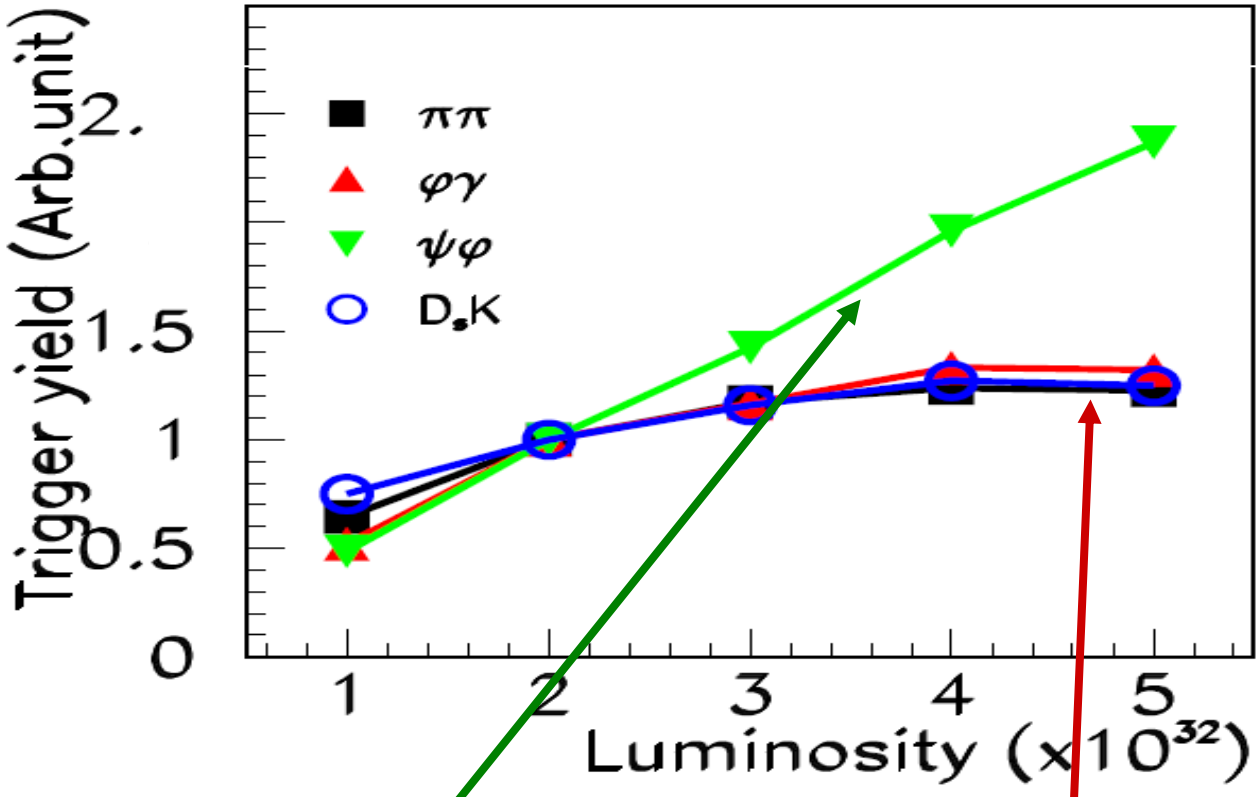
LHCb Trigger System

Existing 1st Level Trigger 1MHz readout

- Veto on multiple interactions
- Existing Trigger based on:
  - High p_T Muons
  - Calorimeter Clusters

Require Displaced Vertex Trigger At 1st level

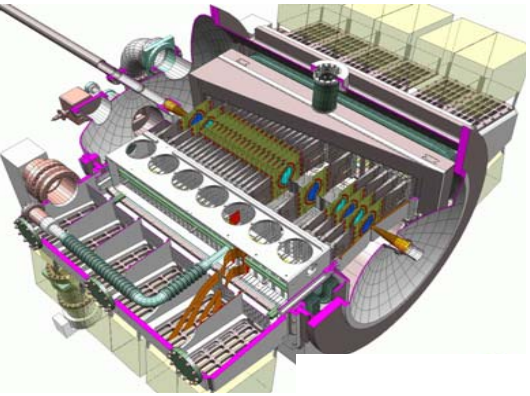
Current 1st Level Trigger Performance



Events with muons – trigger efficient

Events with hadrons – need improved trigger

Radiation Hard Vertex Locator

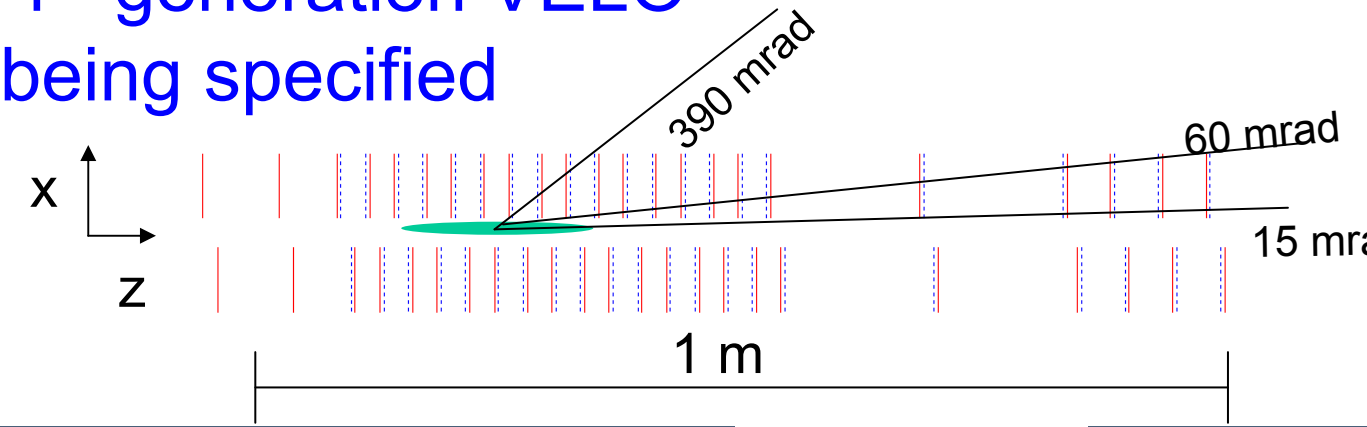


Active Silicon only
8mm from LHC beam
In vacuum

Upgrade Requires high radiation tolerant device

$>10^{15}$ 1 MeV neutron$_{eq}$ /cm^2 per year

n-on-p strip detectors
Enhanced version of 1st generation VELO
40MHz readout chip being specified



Conclusions

- The upgrade programme for the LHC poses severe challenges for the tracking detectors
- Issues of radiation tolerance can probably be solved for all but the most innermost vertexing layer (which may need to be replaceable)
- Issues of granularity requirements increase dramatically the channel count and this leads to many of the biggest problems
- Powering, cooling and services are likely to represent some of the most difficult areas to address
- Limitations of working within an existing detector compound many of these issues
- New technologies are being investigated for sensors, electronics and electronics integration, data transmission, control systems, power distribution, cooling, mechanical support and engineering, data acquisition, triggering and data handling
- Costs of adopting advanced solutions also need to be addressed
- Nevertheless, a huge amount has already been achieved.