Ongoing Pixel developments: A very partial summary

LHC

- We can identify 3 different regions to match radiation damage and occupancy in the current LHC detector

R	Φ	Technology
>50 cm	10^{13}	p-on-n strip 500 μm thick, high resistivity (≈5 KΩ·cm), pitch ~ 200 μm
20-50 cm	10^{14}	p-on-n strips 320 μm thick, low resistivity (≈2 KΩ·cm), pitch ~80 μm
<20 cm	10^{15}	n-on-n pixels 270 μm thick sensors low resistivity (≈2 KΩ·cm) oxygenated

SLHC

- Radiation fluence increases by about a factor of 10 from one region to the other and by a factor of 10 between LHC and SLHC.

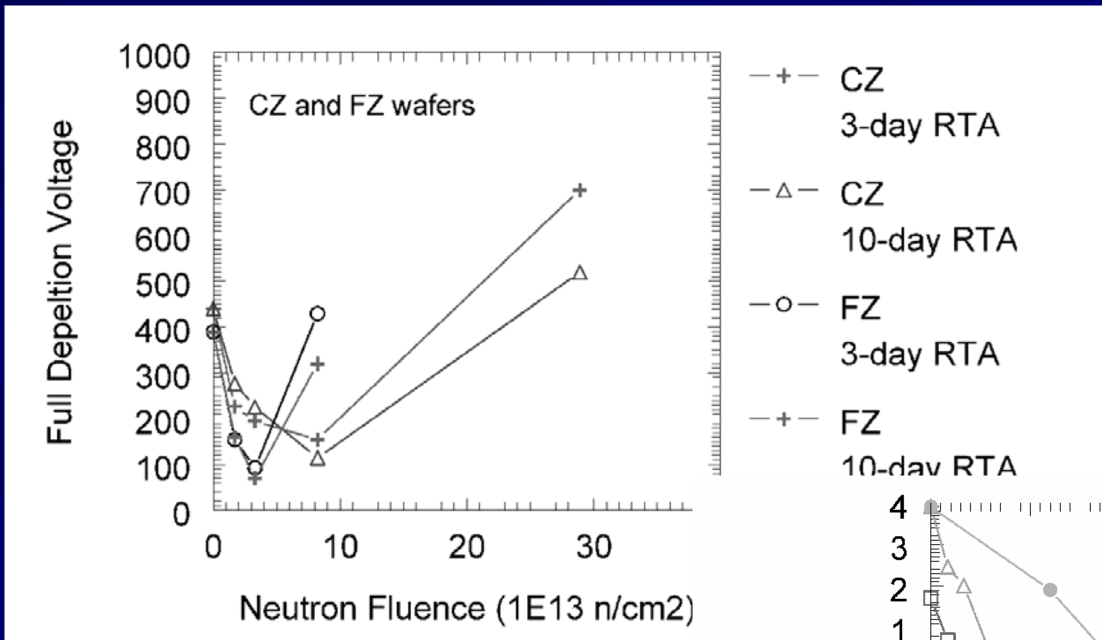
R	Φ	CCE	Technology
>50 cm	10^{14}	20ke	Present rad-hard technology (or n-on-p)
20-50 cm	10^{15}	10ke	Present n+-n LHC pixel (or n-on-p)
<20 cm	10^{16}	>5Ke	RD needed

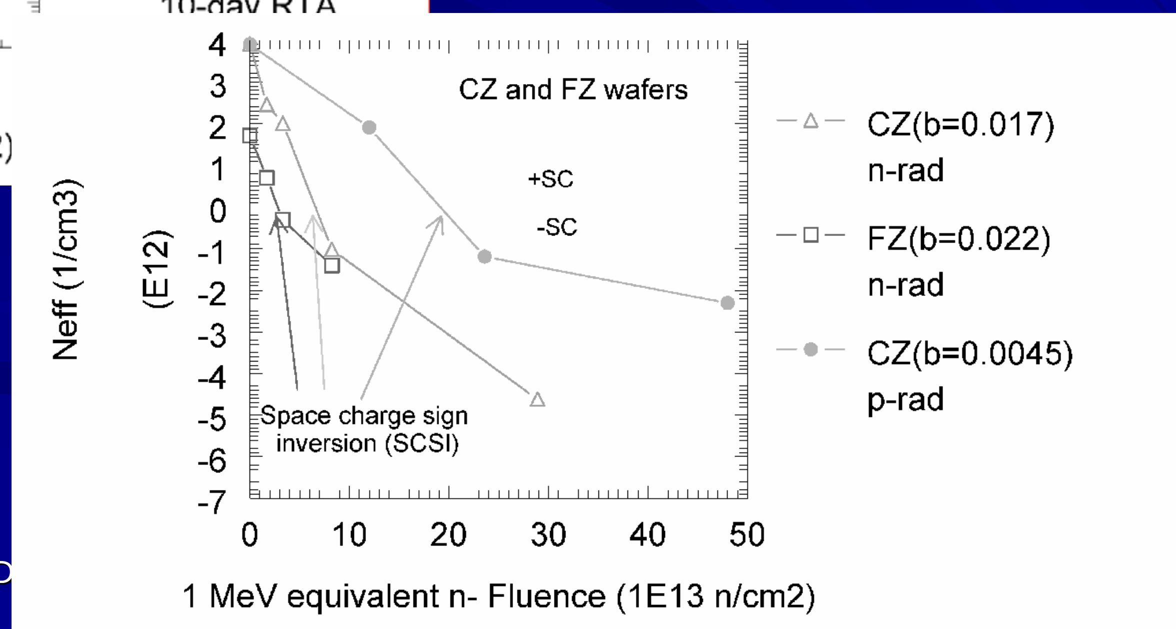
Pixel R&D is complex

- Complicated ROC
- Few groups have in house bump-bonding facilities (PSI and UC-Davis)
- Bump Bonding vendors are costly
- Current activities are very detector dependent
- A lot of pixel developments for LC: DEPFETs, MAPS, FAPS etc.…

MCz silicon

- MCz promises to be more rad hard than FZ



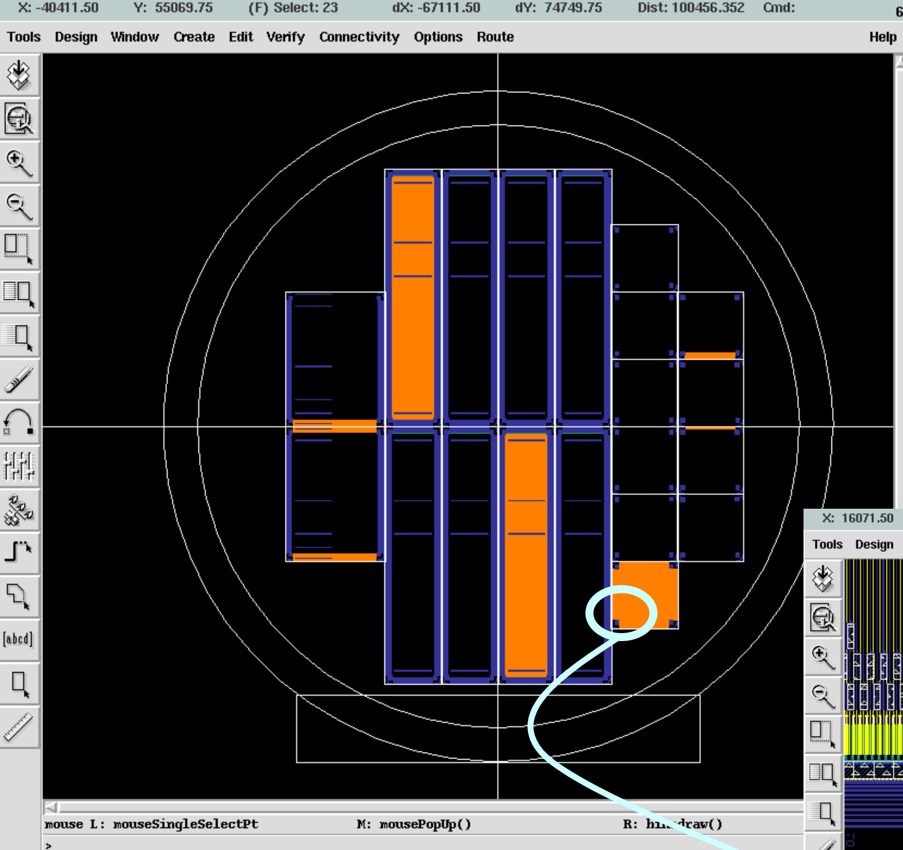


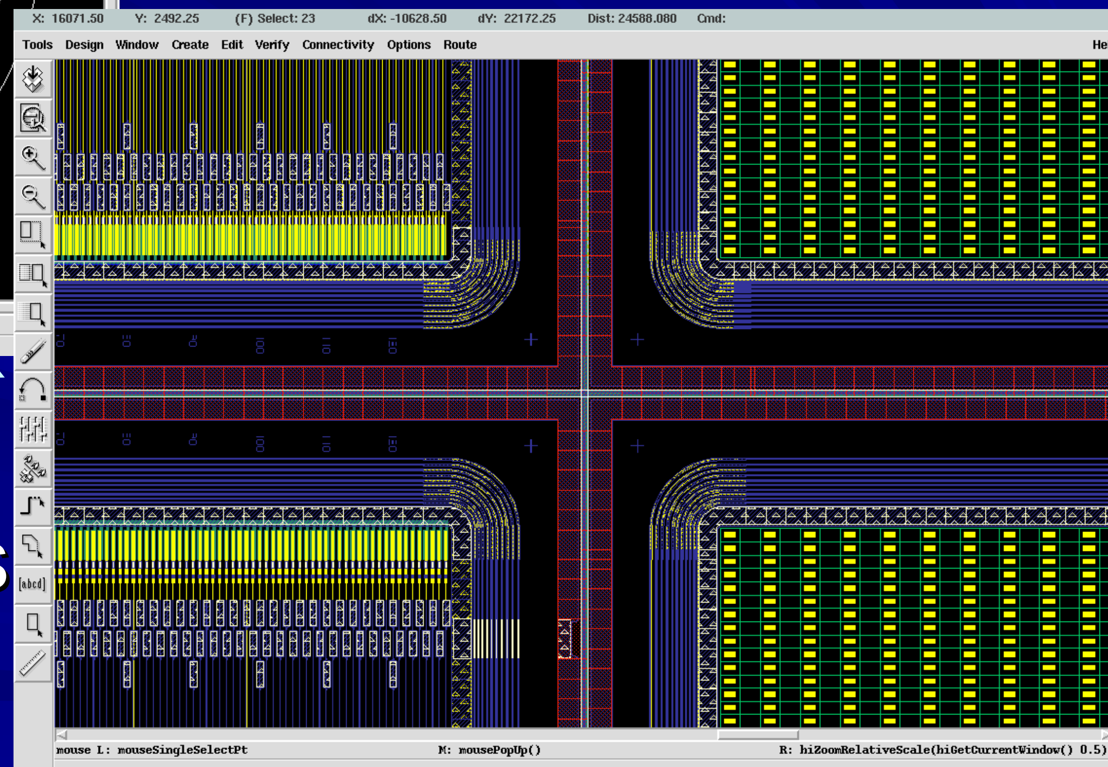
MCz and thin sensors

- Purdue is processing 5 MCz wafers (thanks to M. Moll and Jaakko) with Sintef using CMS/ FPix masks.
  - Allows easy comparison of FZ, DOFZ and MCz.
  - Sensors have standard CMS FPix design
- Purdue, Rochester and BNL are processing MCz wafers containing pixel and strip sensors at BNL. Some of the strip sensors have the CDF-L00 layout
- Purdue is processing thin wafers with Micron (150 µm -200 µm)

BNL wafer

Designed
by G. Bolla

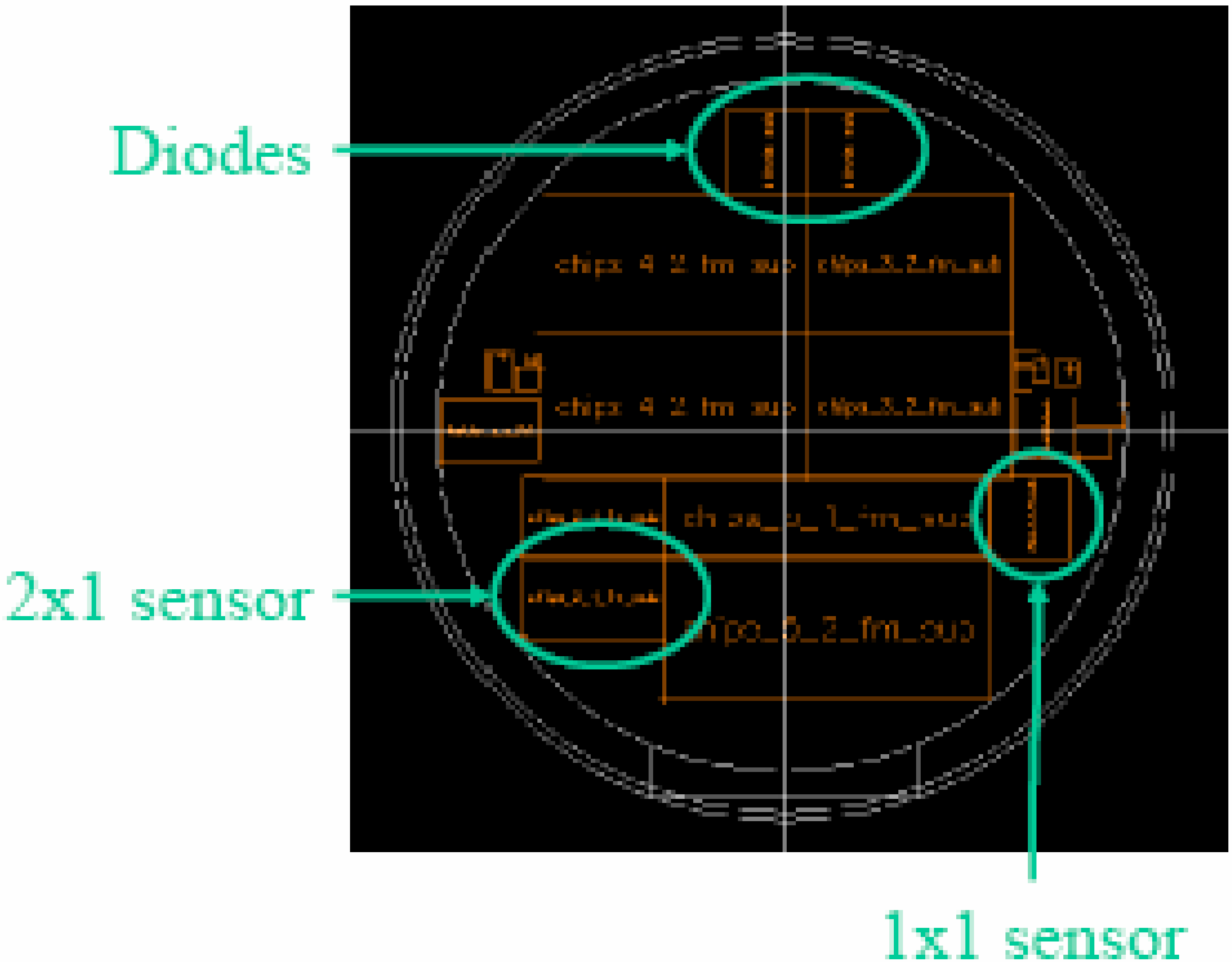




- Mask design in process. Detectors available in about 6 months

Designed
by G. Bolla
and K. Giolo

SINTEF wafer

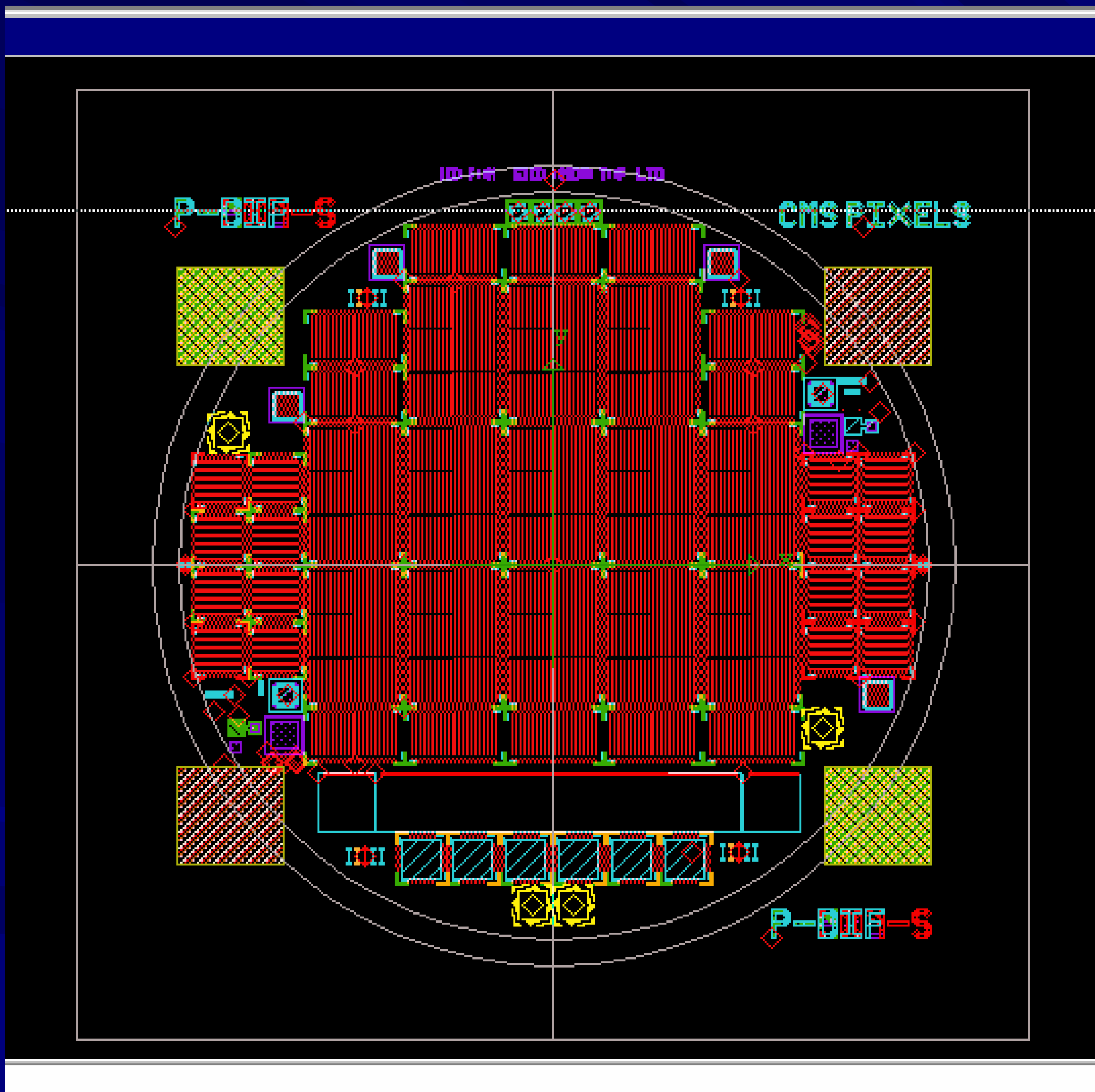


Detectors delivery expected on September 1

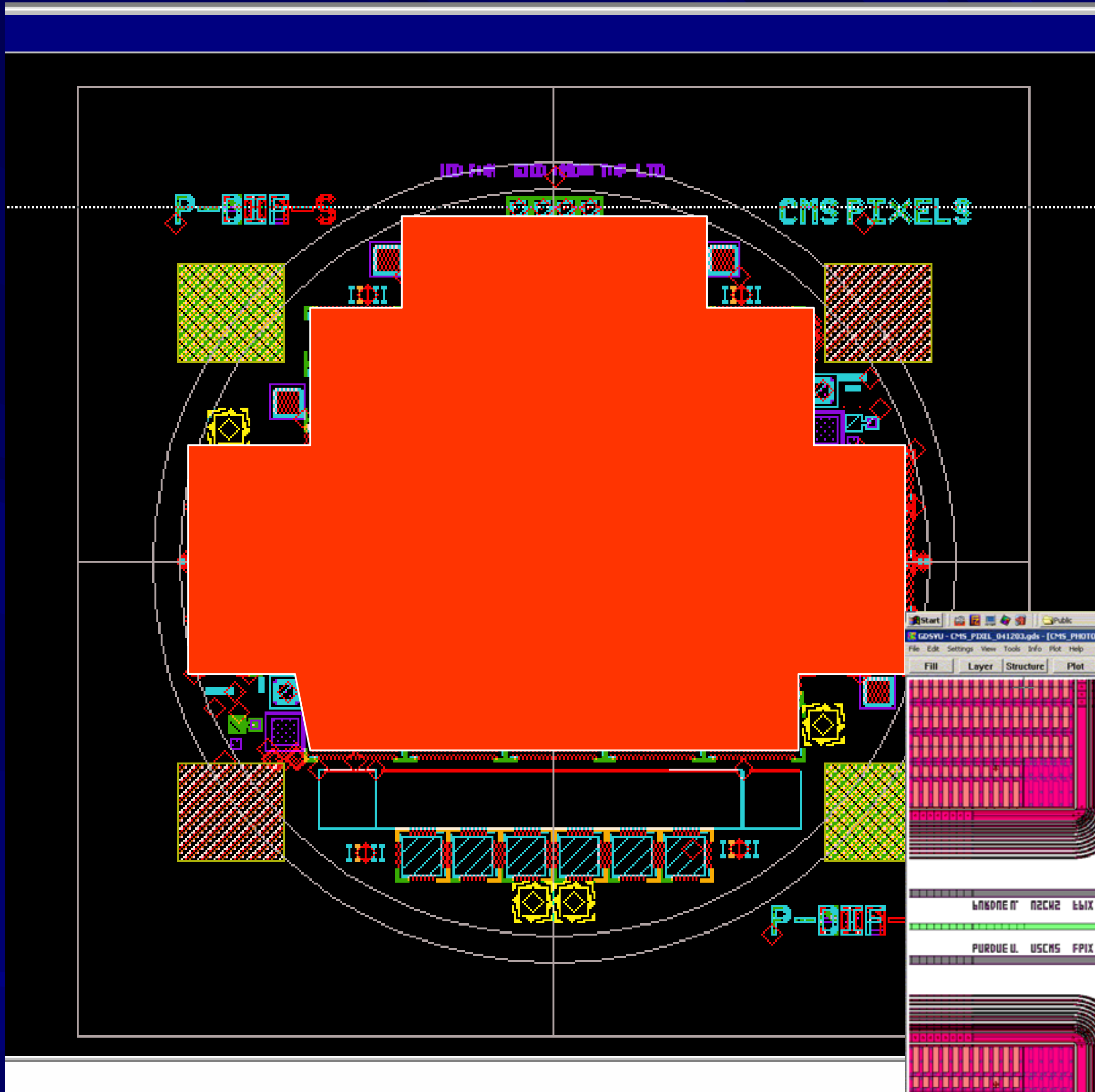
Thin silicon R&D

- We have received thin silicon strips sensors (fabricated with CDF-L00 masks)
- We will compare: 150, 200 and 300 μm thick strip detectors
  - DC measurements
  - Performance studies using the SVX4 chip developed for the so called "run 2b " of the Tevatron
- Pixel masks have been designed. Each 6" wafer will contain:
  - Several pixels sensors matching the CMS ¼ micron chip (100 $\mu m \times$ 150 μm) developed by PSI
  - RD50 PAD structures for SLHC
  - Test structures to study bump bonding
- Pixel sensors should be available for first tests in about 1 month.

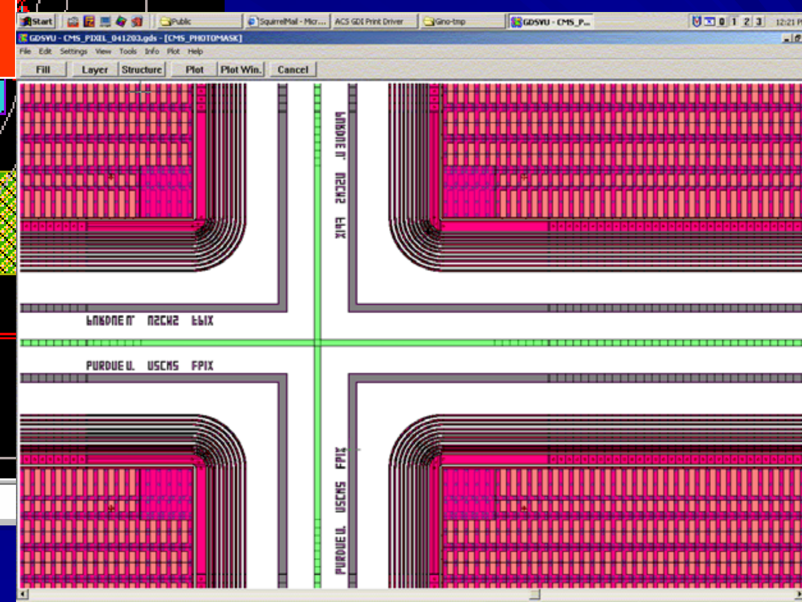
Thin Pixel Mask Layout

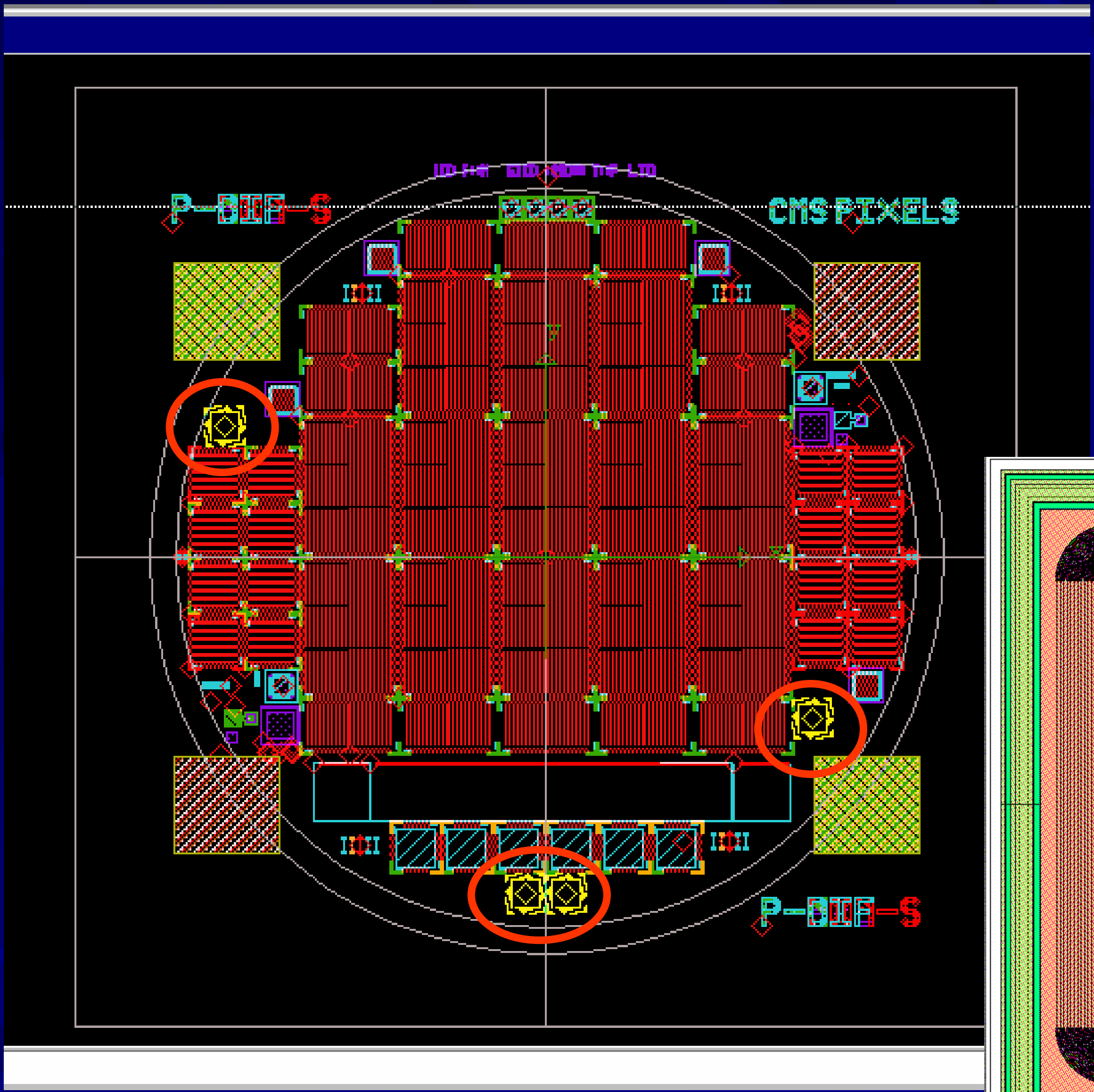


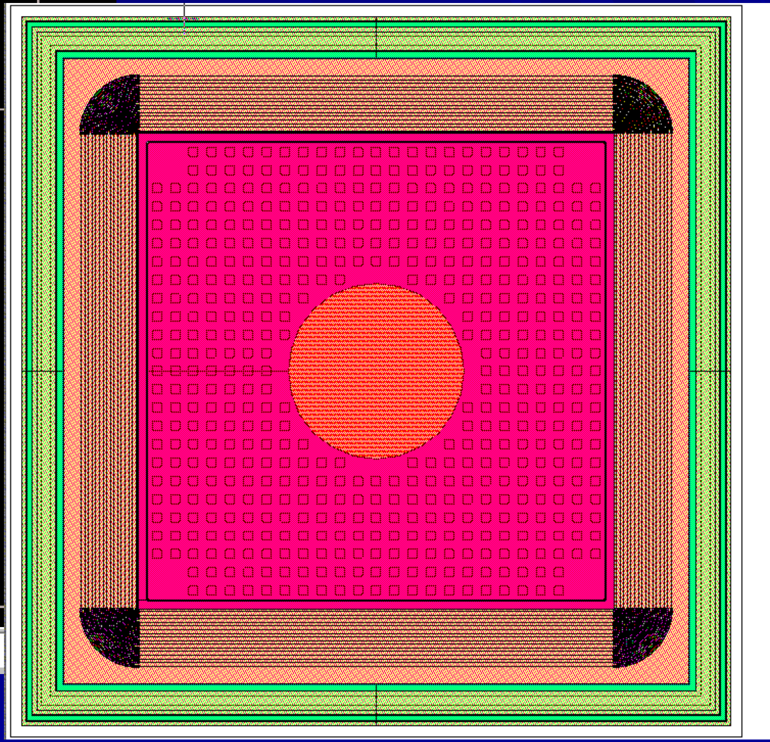
- Masks (6”) are fabricated and processing (oxygenation) started in January.
- Devices should be available in ~ 1 month



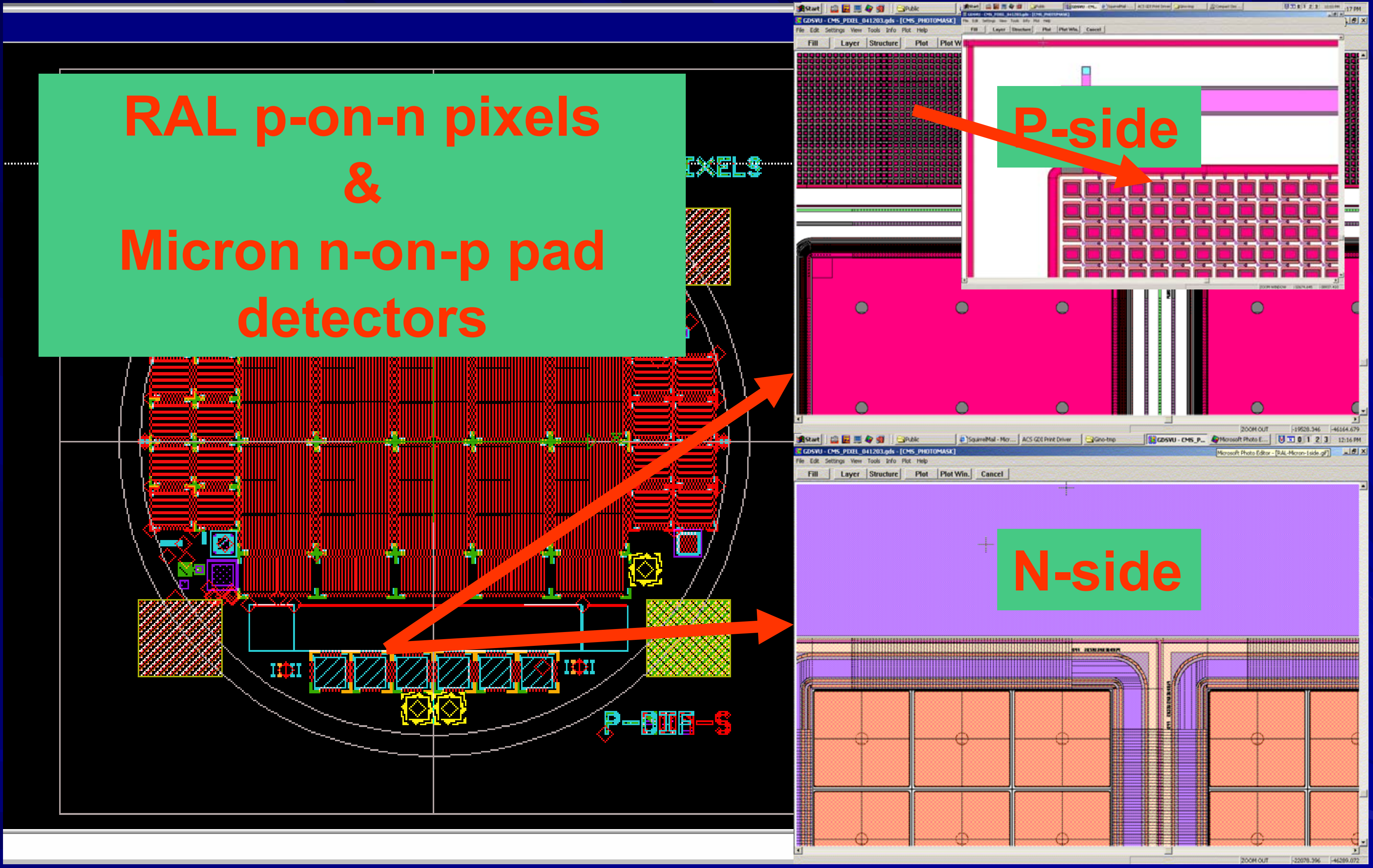
Area is dominated by CMS pixel devices compatible with the 0.25 μm chip



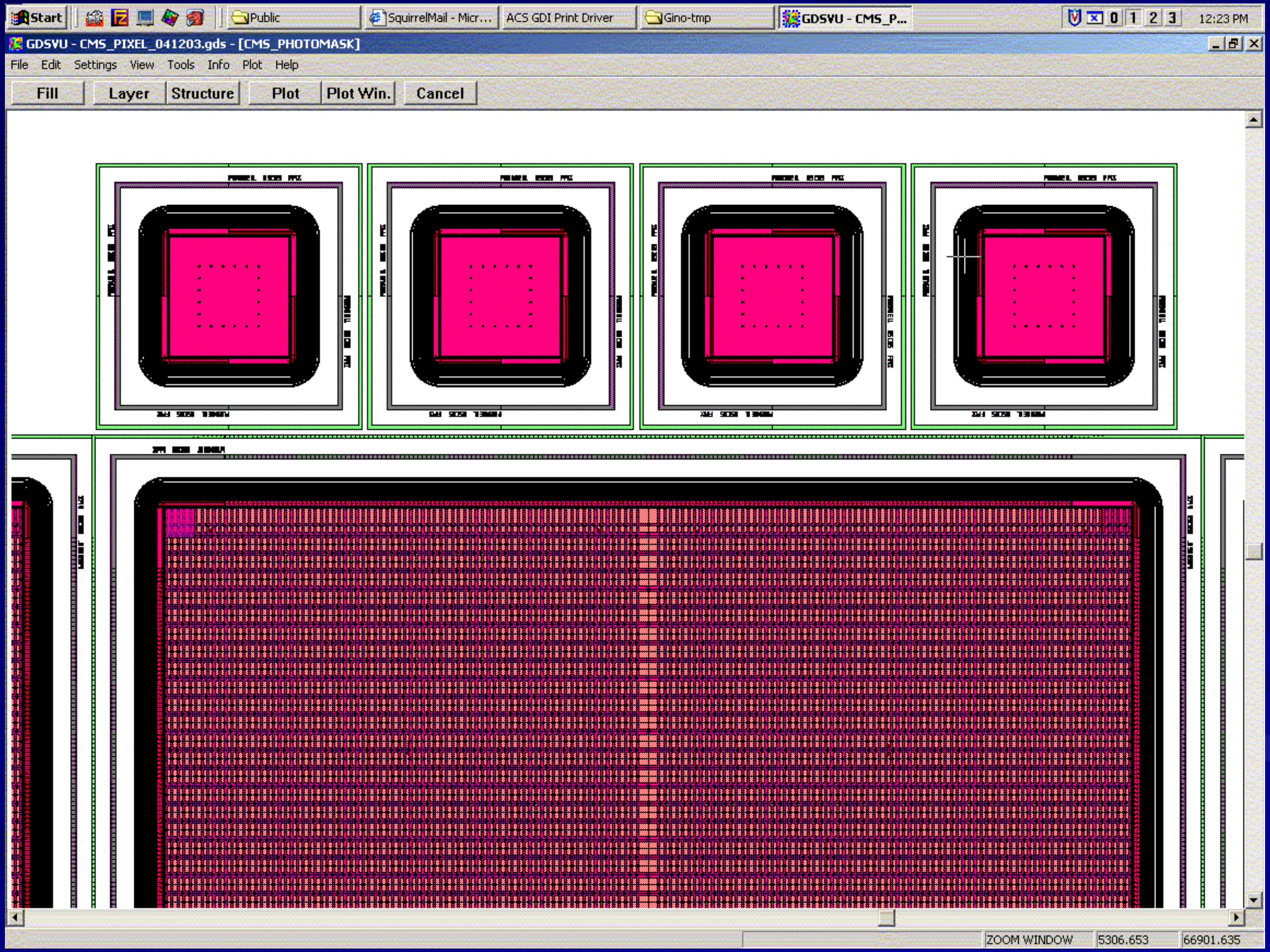




Circled in red the RD50 structures (diodes)


RAL p-on-n pixels
&
Micron n-on-p pad
detectors
P-side
N-side
P-DIF-S

As usual diodes and other test structure for process control



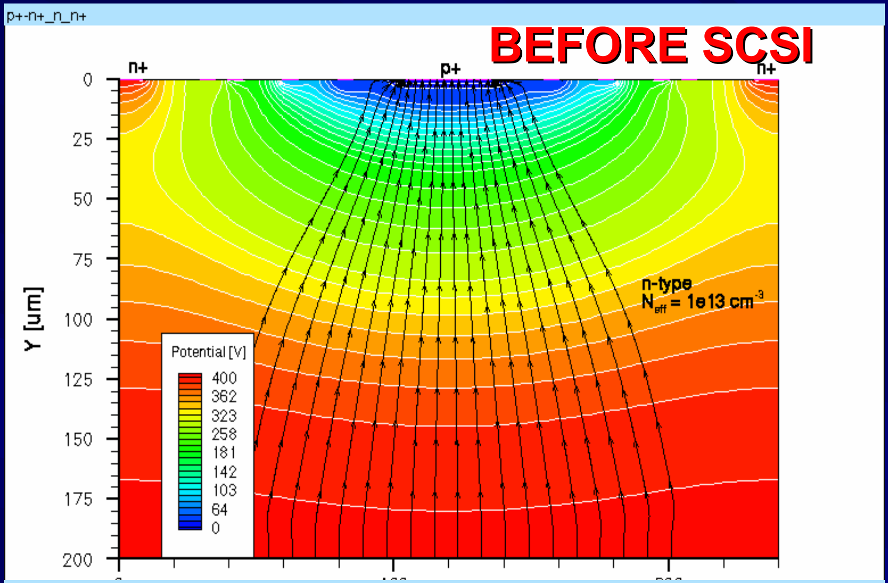
Other activities

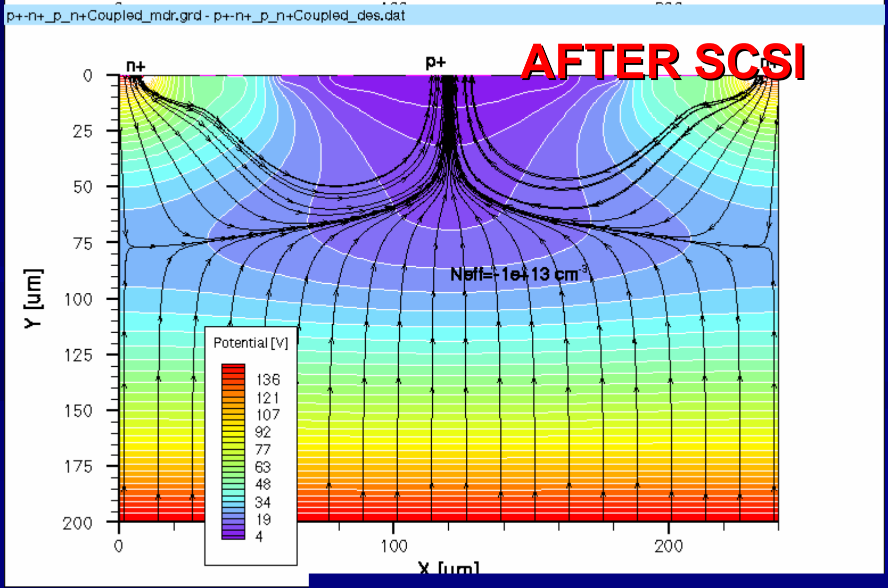
- S. Parker is fabricating pixel sensors for several projects
  – planar/3D active edge for NIH protein crystallography project
  – full 3D active edge for Atlas beam test.
  – TOTEM beam test and high-speed pulse tests with the CERN fast 0.13 micron transimpedance amplifier (Anelli, Jarron, et al.) use full 3D active edge sensors connected to strip readout.

Other activities

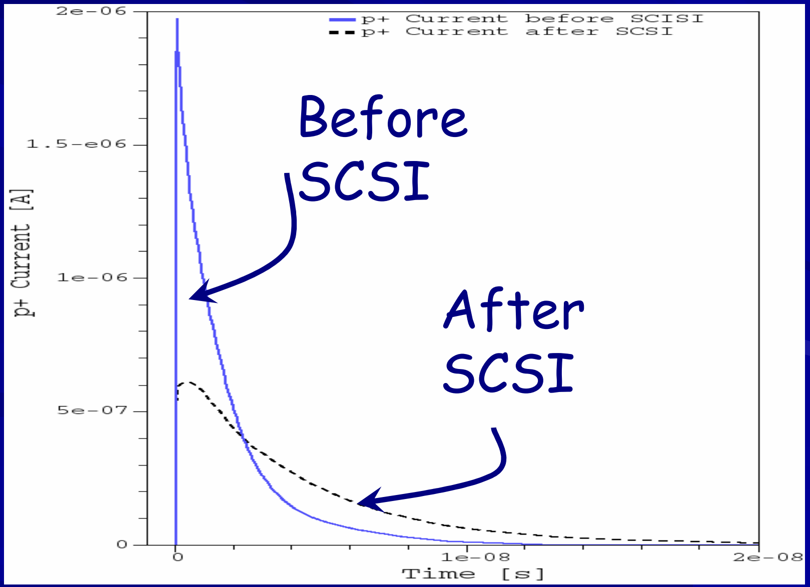
- Several groups are performing pixel simulation:
  - Syracuse, Purdue and JHU (see M. Swartz talk)
  - Uni Zurich (M. Chioggia), PSI, Milan (see T. Lari's talk)
- Aim at comparison between simulation of charge collection properties of different technologies at various irradiation level with experimental data.
  - **Syracuse: BTeV R&D project**
  - **JHU and Purdue: CMS**

Simulation p+- n+ /n /n+





- Use ISE-TCAD
  - Before irradiation: $N_{eff}=10^{13}$ cm^{-3}
    - V_{fd}= 400 V, CCE~98%
  - After radiation: Neff= -1×10^{13} /cm^3 ($\phi=5\times10^{14}$n/cm^2)
    - V_{fd}= 150 V, CCE: 91 %
    - Larger fluence ⇒ increase of collection time.



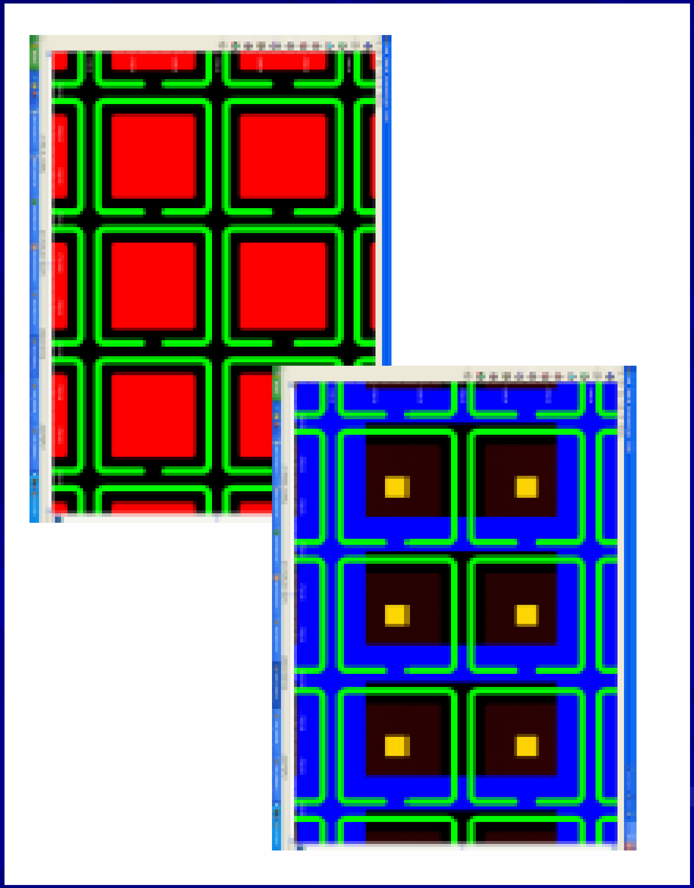
Nabil Menaa Syracuse and J. Miyamoto, Purdue

CCE measurements

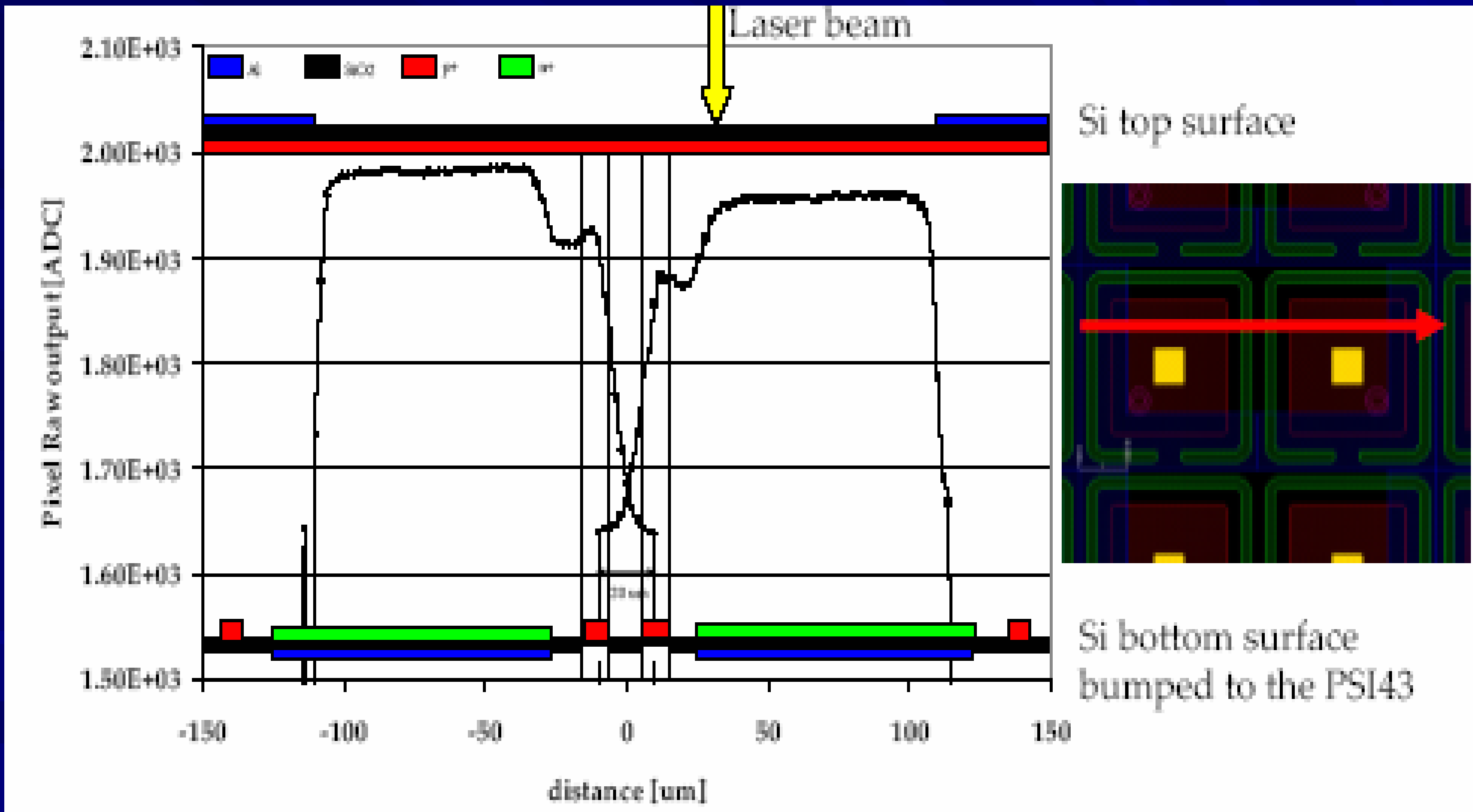
- Beam test area is now working at Fermilab.
- Laser measurements at Purdue and Fermilab
  - **Use 1064 nm laser to study the CCE of pixel systems**
  - **Beam size about 10 μm**

Sensor Geometry

- Implanted n+-pixel (metalized)~98%
- P-stops rings 8μm wide with 12 μm gaps
- Metal grid on the p-side
- Contact between the Al and n+ pixels



Laser Scan



Laser beam
2.10E+03
2.00E+03
1.90E+03
1.80E+03
1.70E+03
1.60E+03
1.50E+03
Pixel Raw output [ADC]
-150
-100
-50
0
50
100
150
distance [um]
Si top surface
Si bottom surface
bumped to the PSI43

Design and test of innovative CMOS pixel detectors

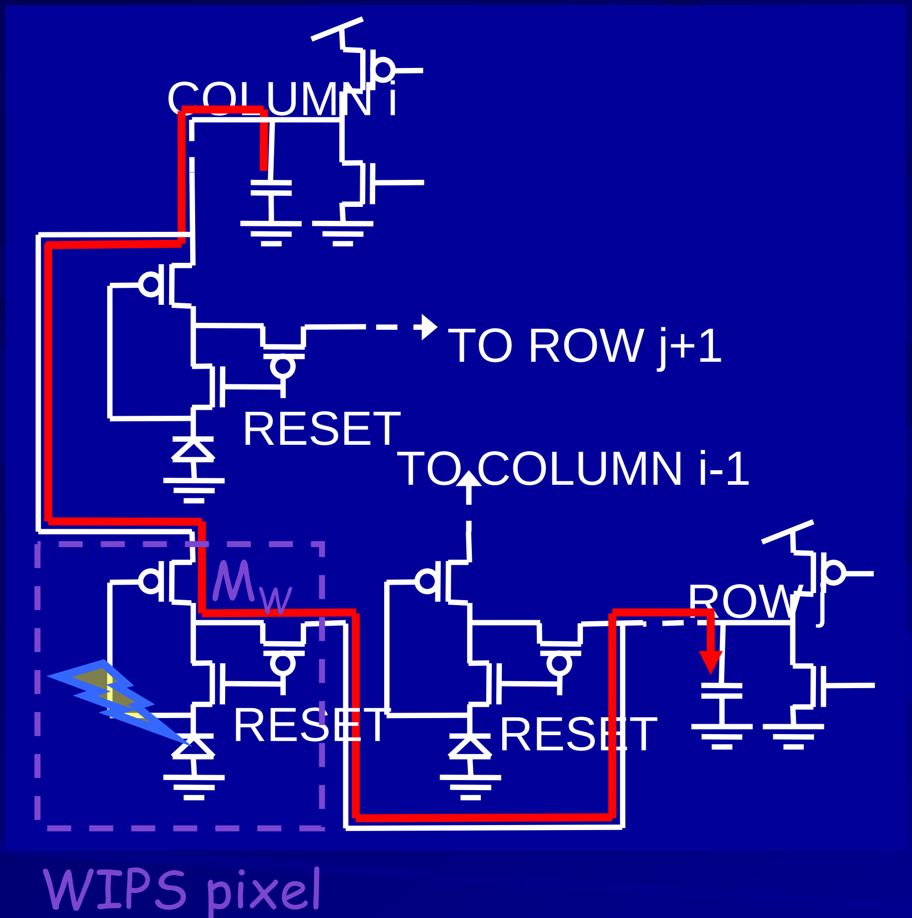
D. Passeri[1, 2], P. Placidi[1, 2], M. Petasecca[1, 2], P. Ciampolini[1,3], G. Matrella[1, 3], A. Marras[3], G.M. Bilei[1]

(1) Istituto Nazionale di Fisica Nucleare
Sezione di Perugia – Italy

(2) Dipartimento di Ingegneria Elettronica e dell'Informazione
Università degli Studi di Perugia - Italy

(3) Dipartimento di Ingegneria dell'Informazione
Università di Parma - Italy

WIPS architecture

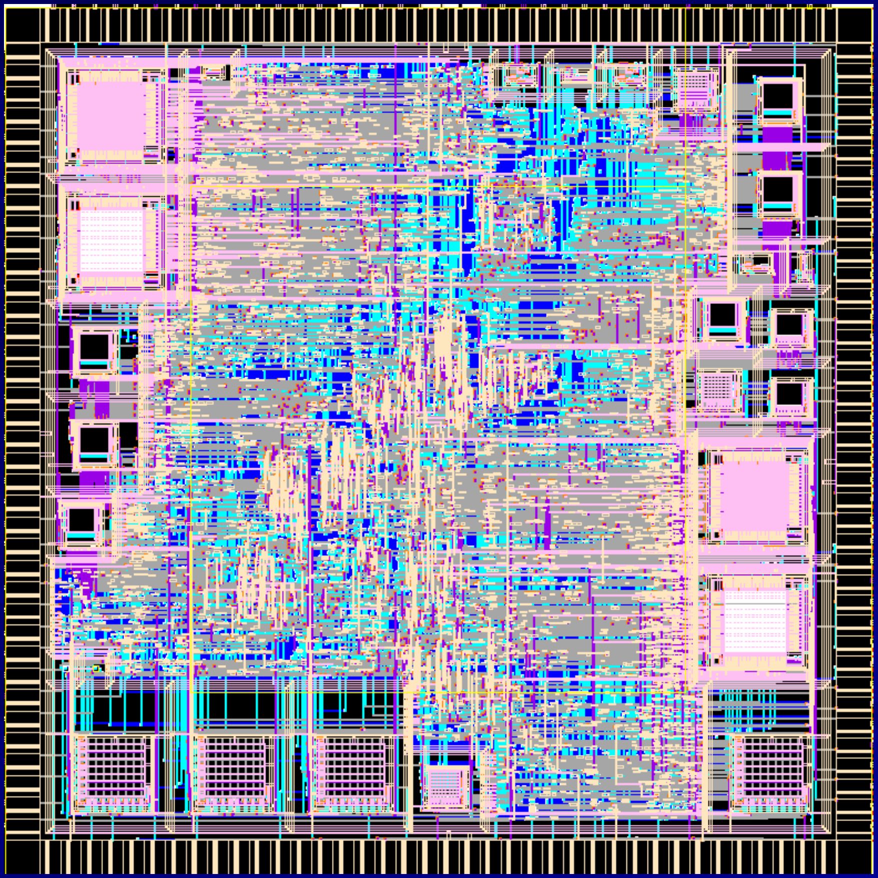


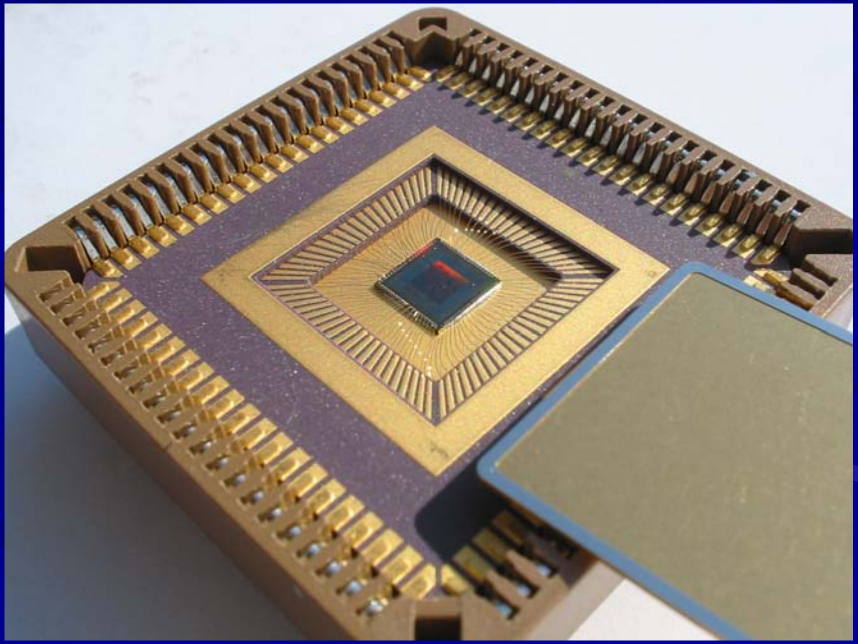
- Pixel architecture 2 PMOS 1NMOS + N-well Diode
- Internal gain ~ 10
- WIPS = Weak Inversion P-MOS
- Pixel area 10 $\mu m \times \mu m$
- Dead Area 15%
- Signal =70-80 mV/MIPS
- ΔT(readout)=$2N_{CLK}$
- N_{CLK}~10 MHz

RAPS01 chip

Designed and fabricated in a commercial 0.18 μm CMOS technology

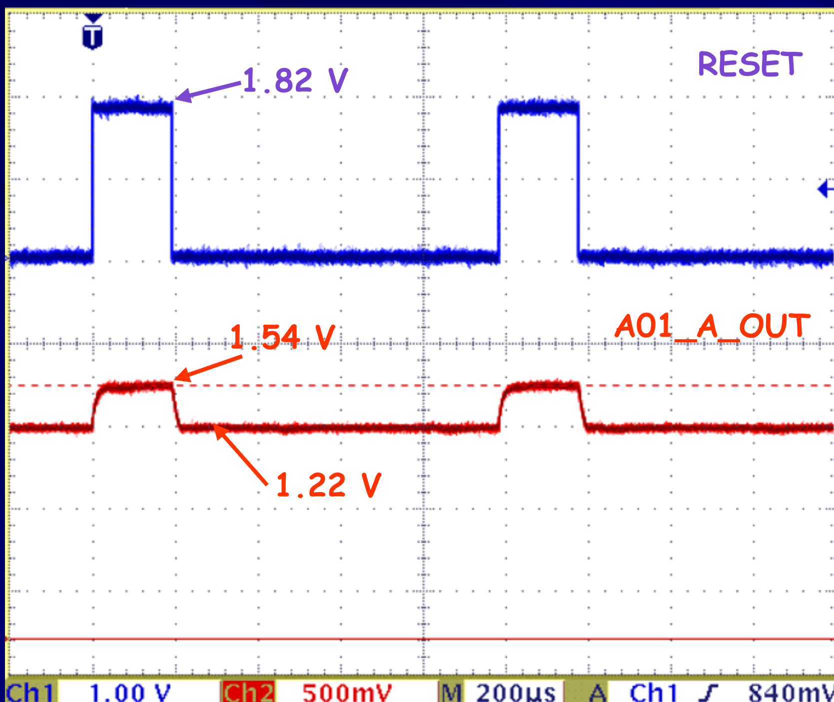
- 11 APS arrays
- 8 WIPS arrays
- test structures
- open-lid, JLCC84 case
- 2 bonding schemes



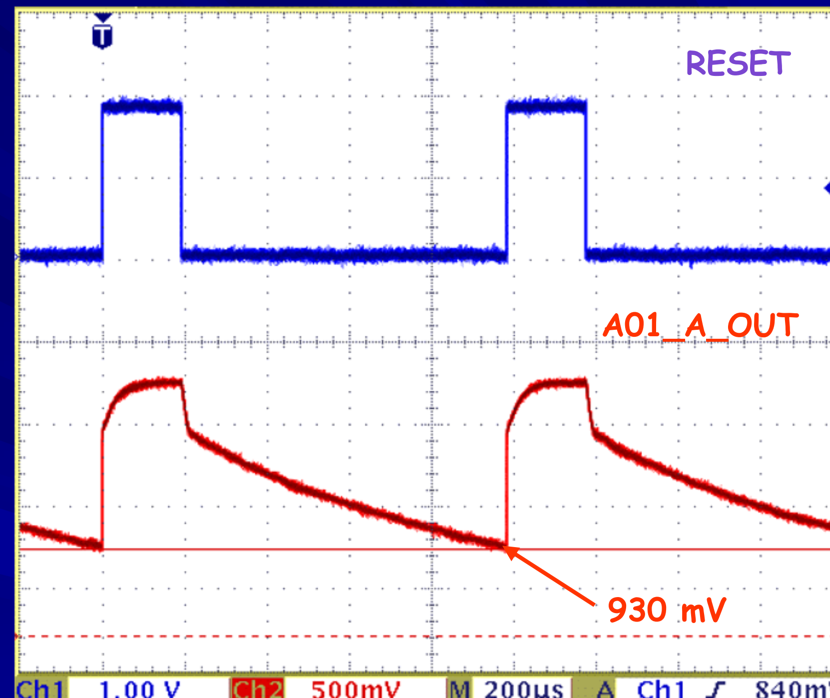


Test results (1)

APS preliminary results



Pixel (0,0), Array 01:
dark condition response



Pixel (0,0), Array 01:
light response

The RAPS experiment

- Preliminary test results on RAPS01:
  - both pixel schemes functional
  - promising performance
- Extensive test to be completed:
  - statistical characterization
  - dynamic performance
  - spatial resolution
  - beam test
- RAPS02 chip:
  - performance tuning
  - more effective exploitation of sparse-reading features
  - on-chip signal processing

Conclusions

- Many groups are interested in pixel development.
- Possible overlap with active pixels developed for LC applications
- The RD50 pixel subgroup is just started and we are still finding out about different activities.