## CMS Compact Muon Solenoid Super LHC: Detector and



### **Electronics Upgrade**







- Brief overview of present CMS Tracker
- Requirements for SLHC
  - Try to identify most important issues
- What have we learned so far from design and development of the Microstrip Tracker?
  - pixels: still in an earlier phase
- Many questions
  - Too soon for real conclusions





- Two main sub-systems: Microstrip Tracker and Pixel Detector
  - Microstrip Tracker comprises 3 (topological) regions



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### Module components



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### Module types

~16000 modules (including spares)

to be produced over less than 2 years.

26 different types of modules in various combinations:

- 14 types of sensor masks
- 24 types of pitch adapters
- 3 types of hybrid layouts (but assembled differently with 4 or 6 APV chips, connector orientation up or down)
- 19 types of frames (e.g. different mechanical assembly jigs)

Very complex nesting of parts.



Pixel Detector designed 6 years ago with many speculative issues and unproven technologies

Today: Technology realistic & feasible

• 3D --tracking points



• replace layers after 6x 10<sup>14</sup>/cm<sup>2</sup> (assumed at the time for TDR)

LAYERS: r = 4.3cm 7.2cm 11.0cm → Area Barrel = 0.78 m<sup>2</sup>  
Disk = 0.28 m<sup>2</sup>  
Total ~ 1 m<sup>2</sup>  
Fluence&Rate  
limited → 
$$r_{min}$$
 →  $r_{max}$   
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#### Silicon microstrip tracker

- ~210 m<sup>2</sup> of silicon, 10M channels
  - 75000 FE chips, 40000 optical links

### Silicon sensors - main parameters

- Substrate: <100>, n-type float-zone, phosphorus doped
- p-side readout, AC coupled, with poly-Si bias resistors
- 500µm 19100 units, 8 designs 3.5-7.5kΩ.cm
- 320µm 6450 units, 8 designs 1.5-3.0kΩ.cm
- $V_{depletion} < 300V V_{breakdown} > 500V$
- Defective strips < 1%. Rejects in modules < 2%</p>

Tender required companies capable to deliver >50% of requirement





- Major areas for discussion
  - Physics requirements
  - System issues
  - Electronic issues
  - Sensor issues
  - Mechanical issues omit for time reasons
- Pixels will be more important at SLHC
  - rather key point...
    - since pixel technology is not yet proven on large scale





- Even more intense radiation environment
  - "only viable solution is to completely rebuild Inner Detector systems..."
- Working group concluded three tracker regions
  - R > 60 cm push existing technology ie microstrips
  - 20 < R < 60cm further developed hybrid pixels
  - R < 20 cm most likely new approaches required</p>
- This probably does mean three trackers!
  - plus topographical divisions?
  - could need much larger community
- New CMS requirement provide tracker data for L1 trigger
  - Major new challenge

# **Schedule for LHC Upgrades**



**Peter Sharp CERN** 

**CMS Electronics 2003** 





### Higher luminosity and (eventual?) higher CM energy

- L => 10<sup>35</sup> cm<sup>-2</sup>.s<sup>-1</sup> E<sub>CM</sub> = 28 TeV
- NB Strong correlation between L and beam lifetime
- Expect to be guided by LHC discoveries and success of machine operation
  - Electron and muon track reconstruction will still be important
  - Rarer channels to be studied?
  - More energetic jets with more particles and higher track density
  - Higher granularity will evidently help

- but

No of channels, power & material budget are major concerns

### What will remain the same?



- Specifications no obvious reason for major change
  - momentum & spatial resolution
- Volume available
- Space & cooling in control room & cavern is also limited
  - increased off-detector electronics must be compensated by density
  - total power constraints will also not relax much
- Ability to cool system
  - No dramatic breakthroughs expected
- Budget?

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Should expect it to be a constraint

## What will not remain the same?



- Number of channels will increase
- Detector (sensitive) thickness and material *might* change
- Electronic technology changes are inevitable
  - and we are forced to follow them
- Off-line computing power will increase... as will...
- on-detector (ASIC) processing
  - limited by power dissipation
- off-detector (FED) processing
  - may be limited by increase in channels and complexity of data

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CMS has pioneered automated module assembly

- Almost fully proven, and module assembly is now going quite fast
  - 15000 in ~2 years

### But

- Significant development time to reach this point
- Many crucial, detailed, labour intensive tasks
- Some problems still occurring
- System assembly, installation and commissioning still ahead
  - Much less adaptable to automation
- SLHC tracker will be different more modules &...

### How much time is needed?



- For present system R&D started in ~1990
  - we did not understand electronic technologies as well as today
  - much time was spent on sensor development
- Where were we 5 years ago? (early 1999)
  - Sensors: MSGCs and silicon
  - Readout ASICs: 0.25µm had begun
  - Optical links: well advanced but much done since
  - Hybrids, power, readout: barely started
  - Module assembly: automation demonstrated
- December 1999

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- MSGCs abandoned despite much progress
- 0.25µm CMOS adopted as baseline technology





### 5 years is not a long time

- Some things have taken longer than we expected, even when we thought we were finished
- We underestimate time for R&D to reach maturity
  - "90% of effort on last 10%"
  - especially affects evaluation and qualification





- Possible date for upgrade 2015
  - for some assumptions see earlier slide
- Possible schedule including contingency
  - 5-6 years R&D, depending on start, funding & people ramp
  - 2 years qualification of components in systems
  - 3 years construction
- Start date and funding are crucial assumptions!!



- Analogue readout was a good choice
  - but may need to reconsider digital for the future
- Optical data transmission (analogue) a big success
  - but links are the largest part of the electronics budget
- Investigating major design variants is lengthy and costly
  - often introduces new features, needing verification
- Radiation tolerance

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- Qualification is time consuming (x-ray systems & SEU)
- Automated testing
  - successful, but needs much preparatory effort & tools

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- Manufacture now looks safe (but...!)
  - Large, complex boards are challenging
  - Special components (optical Rx, TTCrx,...) need care
- Processing power will increase
  - but constraints are harder to anticipate
- Components evolve fast (~5 years lifetime)
  - Functionality increases and design time
  - Technology changes Pb free solder (2006), fpBGA assembly,...
  - Power is hard to predict reliably until design is well advanced

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### 0.25µm CMOS probably available until ~2009

- 0.18µm and 0.13µm already available
  - essential design tools are increasingly complex
- 300mm wafers next standard, already in use
  - implications for bump-bonding & other equipment, eg probers
- Supply voltage reduction (0.13µm 1.2V/1.5V)
  - challenge for design dynamic range
  - trend to higher speed and lower power applications
    - not necessarily at the same time
- More digital logic possible in smaller area
  - programmable functions to tune, correct, test, debug,...

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- Radiation tolerance and noise
  - Iook excellent without special design tricks
    - but care over details still required
  - SEU rate will be more of an issue

- Cost significantly higher entry cost
  - how to plan development & NRE? under discussion
  - but wafer costs probably scale with area, or even decrease
- Availability of engineers is a major concern



### Simple assumptions eg. supply voltages scale, 80MHz

- Scaled APV-type circuit (M. Raymond)
  - ENC ~ 700e for 2cm microstrip (+ leakage current)
- power/channel : 2.3mW (0.25µm) => 0.4mW (0.13µm)
- Good news!!

### but

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- No of channels probably scales similarly...AND...
- Power in cables increases
  - $P_{delivered} = P_{FE} + I^2 R_{cable}$  and  $P_{FE} = IV_s$
  - V<sub>s</sub>(0.13μm) ~ 0.5V<sub>s</sub>(0.25μm)
  - $P_{cable} = R_{cable} (P_{FE}/V_s)^2$   $R_{cable}$  likely similar to present value





- Radiation levels
  - x5(?) LHC realistic allowance for machine performance
- Performance
  - Series noise (C<sub>det</sub>) may decrease but parallel (I<sub>leak</sub>) may not
- Power dissipation
  - Ieakage current increase could dominate module power?
- Manufacturability & R&D
  - will unusual materials be acceptable?
  - are they available in required quantities?
  - any special processing requirements?
  - close collaboration with major manufacturers from early stage





### Sensor material

- silicon is still most robust, well understood and reliable material
- no breakthroughs apparently (!) imminent ...??
- R&D on new materials takes much time (+ \$\$\$) to mature
- therefore ...
- even innermost region still likely to be silicon?
- if this is not true...
  - need quickly to demonstrate alternatives and R&D required
  - must be capable of reaching maturity in 5-7 years
  - Iarge scale, commercial manufacturing is essential
  - evaluate funding needed to bring to maturity



- use 5x TDR fluencies
- old fluence limit of  $6 \times 10^{14}$ /cm<sup>2</sup>  $\rightarrow$  r<sub>min</sub> ~ 26cm !! Problem!
- What can we do?
  - Change detector more often
  - Improve fluence limit off sensor
- Need to study sensors more !
  - $\rightarrow$  RD50







- Double sided processed,  $n^+$  on  $n silicon \rightarrow expensive but high quality detectors$
- So far many investigations for fluences ~  $1x \ 10^{15} \text{ cm}^{-2}$ , still quite ok!
- Reduced signal collection  $\rightarrow$  partial depletion depth  $\rightarrow$  trapping
- Partial depletion depth controlled by High voltage capability
  - Oxygenation
  - Czochralski (lower costs)
  - Epitaxial silicon
  - Thinner detectors (e.g.  $200\mu \rightarrow$  leakage current ??)
  - Reverse polarity ??
- **Trapping** so far not engineerable
- $\rightarrow$  final fluence limit for silicon detectors !!!
- Fluence ~  $3x \ 10^{15} \ \text{cm}^{-2}$   $\rightarrow Q_{IR} = 25\% \ Q_{NIR}$  (very speculative !)

Is this enough signal charge for pixel ROC ?? (benefit from 0.13µ CMOS chips ?) RD50 workshop May 2004 28 Geoff Hall





- Oxygenated CMS pixel sensors
- Double sided processed n<sup>+</sup> on n – silicon 285µ thickness
- CMS Pixel test beam at CERN
   Summer 2003
- Shallow track method for depletion depth studies
- at 450V almost fully depleted
- see trapping !

 $\Phi = 3x \ 10^{15}$  would imply a minimal pixel layer radius ~ 8cm !

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### First conclusions (R. Horisberger)

• Current pixel system could possibly be extended and rebuilt for SLHC operation in a radial region of 8 cm to 16 cm.

• e.g. 3 Layers at: 8cm 11cm 14cm

Pixel System #1

- Silicon sensors could eventually be pushed to a fluence limit ~ 3x 10<sup>15</sup> cm<sup>-2</sup>
- Pixel area stays 15000  $\mu$ m<sup>2</sup>  $\rightarrow$  observe no benefit from smaller pixel
- The pixel ROC's need some modifications to take the enormous data rate





### <u>Conclusions on pixels at intermediate radii</u> (R. Horisberger)

• The use of single sided processed n<sup>+</sup> on p-silicon detectors could give a substantial reduction of the sensor costs.

• With n+ on p detectors partial depleted operation should be possible although high voltage issues at the guard ring region need R&D.

• Substantial cost reductions due to cheap module design decisions could result in module costs of 2100 SFr. With +20% add on  $\rightarrow \sim 100 \text{ SFr/cm}^2$ 

• At this price level it becomes conceivable to cover intermediate radii:

e.g. 2 Layers 18cm 22cm Pixel System #2





• Need to cover the radial region 25cm to 60cm with tracking detectors that can deal with SLHC track rates

• Silicon strip detectors have sensor element area 10mm<sup>2</sup> to 15mm<sup>2</sup>

• For 10x luminosity increase occupancy requires a reduction of sensor element area by factor 10.  $\rightarrow$  Sensor element  $\sim 1 \text{mm}^2 - 1.5 \text{mm}^2$ 

• Propose Macropixel detector with pixel size 200um x 5000um (Strixels)

• Use simple DC coupled p<sup>+</sup> on n-silicon detector and route the strixel signals on thick polyimide (~40µ) insulation to periphery and bumpbond to modified pixel ROC for cost efficient zero suppressed readout.  $\rightarrow$  ~40 SFr/cm<sup>2</sup>

• With this price one can cover probably a 3 Layer system:

3 Layers 30cm 40cm 50cm Pixel System #3

### **Summary** (*R. Horisberger*) L=2500fb-1, Fluence .vs. Radius

- Propose 3 Pixel Systems that are adapted to fluence/rate and cost levels
- Pixel #1 max. fluence system
   ~400 SFr/cm<sup>2</sup>
- Pixel #2 large pixel system
   ~100 SFr/cm<sup>2</sup>
- Pixel #3 large area system Macro-pixel ~40 SFr/cm<sup>2</sup>
- 8 Layer pixel system can eventually deal with 1200 tracks per unit pseudo – rapidity
- Use cost control and cheap design considerations from very beginning.
- Can this be done for 2012/13 ????

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- Discussed in Working Group report
- 1. Those probably meeting *large scale* maturity criterion
  - defect engineered silicon / cryogenically operated silicon
- 2. Those probably not meeting maturity criterion
  - 3-d detectors/ diamond
- 3. Those not mentioned
  - disposable sensors + any other ideas?
- Each solution needs customised electronics
  - Not credible to develop electronics for all options





#### Defect engineered material

- eg Oxygen doped, Magnetic Czochralski
- no special electronic implications, if manufacturers accept processes
  - would probably apply to diamond if large scale production possible

### Cryogenically operated

- Pros: some evidence of improved radiation resistance
- Cons: significant implications for electronic developments
  - no proven solutions based on widespread processes (CMOS)
  - all tests must be done at operating T, equipment not readily available
  - significant performance changes expected not just analogue
  - Iess predictable at present, and time-consuming to prove





- If ultra-radiation hard sensors are not available?
  - possible alternative for innermost region?
  - assumed to be based on commercial electronic technology
    - eg MAPS or a-Si+CMOS
- production cost of disposable sensors probably feasible
  - provided NRE/development costs contained
  - savings on assembly, etc might also be significant
  - Pros: continues trend to industrial-style assembly
  - Cons: which type of sensor and how?
    - need pixel sensor but not labour-intensive
    - handling of activated material



Silicon?

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- SAPV: 2 per die
  - Outputs in middle
  - Power rails bump bond to substrate
  - services via substrate surface
  - service chips at periphery



 But might be candidate for commercial assembly on large scale?

"Straw man" module

Adapt sensor for commercial bump bonding

Is it possible with more conventional assembly?







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Outputs

#1

Signal

inputs

128 x 100µm

staggered

#2

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- Traditionally digitisation, rapid data transfer, off-detector processing
  - very significant changes will be required to adapt tracker readout architectures to trigger requirements
  - pixels are asynchronous, so even more difficult





- a replacement tracker must further develop automation
  - it will be large
  - Iimits on funding, manpower, time, maintenance,...
  - bottlenecks must be overcome early
  - modules must be simplified further endcap remains most difficult
  - could task be sub-contracted?
  - disposable detectors might be necessary
    - but activation and personnel irradiation is a big issue
  - sensors must reach large scale maturity in ~5 years
- If not true, what is the alternative?





- Power will be a major concern
- Material budget should not increase
- Large systems are hard to build
  - Qualification must be taken seriously
- R&D duration is always underestimated
  - Reduce the number of (complex) module types
  - Increase automation of assembly
- Sensors are just one of many issues
- Electronic technology evolution will bring benefits
  - and also much difficult work